TEXAS INSTRUMENTS

SPEECH SYNTHESIZER

THEORY OF OPERATION

PRINCIPLE OF OPERATION

The Speech Synthesizer Peripherial generates synthetic speech within the Synthesizer I.C. (TMC 0285) from coded data stored in Phrase ROM's (PHROMS). The 0285 interfaces to the Home Computer through the Data Bus (D_0-D_7) when a speech select (SBE) is present. The 0285 in turn controlles the PHROMS to fetch data when required. Data brought to the 0285 is fed to the speech synthesis network, there converted to a digital code, then fed to a Digital-to-Analog (D/A) Converter to generate the analog (speech waveforms). The analog output is coupled back through the Home Computer and amplified to drive a speaker.

The TMC 0285 (U1) is a MOS LSI Circuit that contains not only Data and control interface but also complex circuiting that uses coded data strings to generate voiced or unvoiced sounds. These sounds are processed through a digital filter network whose output is converted to an analog speech signal. For a detailed explaination of the TMC 0285 refer to TI Drawing # 1501640 and ELECTRONICS, August 31, 1978, Page 109, "Three-Chip System Synthesizes Human Speech".

The PHROMS are TMC 0350, 16KX8 ROMS. The PHROMS use an 18 bit address of which the 4 MSB's select 1-of-16 PHROMS, although use with the speech synthesizer peripheral is limited to seven due to power constraints.

OPERATION

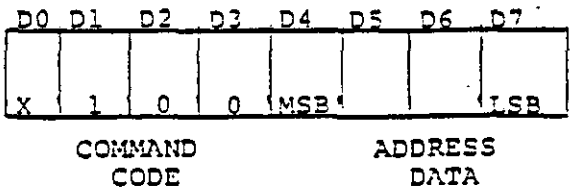
Activity in the speech peripheral is initiatee by the Home Computer CPU through a speech select (SBE). A select could be a Read from the speech module or a Write to it. A Read Select (RS) to the 0285 is decoded through U3 (LS138) from SBE $\overline{A5}$ $\overline{A15}$ (address 9000). A Write Select ($\overline{WS}$) is derived from SBE A5 $\overline{A15}$ (9400). These signals determine whether the TMC 0285 will put information on the Data-Bus or receive information from the Data-Bus. Immediately after a $\overline{WS}$ or $\overline{RS}$ (those signals are active low) the 0285 will take the system not ready (Din-12 of the I/O will be low). It will hold the system not ready until the data being received has been latched (in the case of a write) in or the data being sent is stable on the bus (in the case of a read). The not ready time is around 20μsec but is variable and depends on which mode has been selected and the command. Timing can be obtained from the SPEECH MODULE Spec 1034759.

After receiving a Command the 0285 begins processing it and if required sends the control and data signals to the PHROM. The control signals Io and I1, pins 15 and 16 respectively, one active high with I1 active for an address load and Io active for a data read. Both Io and I1 active is a Read and Branch but is not used in the present system.

Address information is passed to the PHROM's on the Add 1,2,4 and 8 lines, pins 2,25,23,21 respectively. The add 1 is the LSB and add 8 the MSB of the address nibble inputted to the data bus D1 through D4. Data from the PHROM's is transferred to the 0285 serially over the Add 8 line (pin-21) following a Read (Io) function. Transfers are synchronized by the ROM Clock (U1-3) which is a 160kHz (6.25 s) signal. See figure 1.

The ROM Clk is a divide by four of the internal oscillator (U1-6). The oscillator is adjusted to 160 ± 5kHz by clipping R5, R6 or both. The speech output is on U1-8 which is an open drain requiring a D.C. path to 9round (R3). R3 sets an operating point at about one-third supply to prevent clipping the peaks of the audio output. Capacitor C2 provides D.C. isolation and C6 along with R3 forms a low pass filter to the 8kHz sampling rate.

A sample sequence to speak a word assuming its address in PHROM has previously been obtained would be as follows:
The I/O address is set to 9000 (speech write) by the Console, SBE goes high, $\overline{Ws}$ at U1 goes low, and ready (I/O-12_ goes low and takes the console not ready. Along with the address the I/O Data Bus was set up with the command (a load address) and the lease significant nibble (4-bits) of the word address in PHROM, formatted as follows:

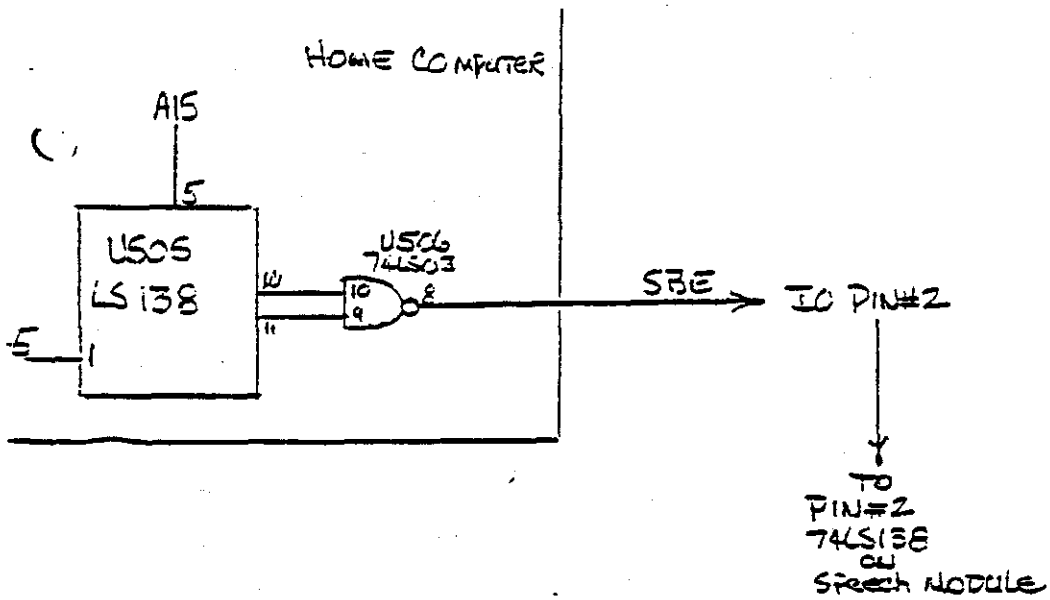


The nibble of address and an I1 pulse would in turn be sent to the PHROM's, U2. Uponcompletion of latching in the data U1 releases the ready line (around 20-25 s) and allows the console to continue. Since the PHROM takes 18 bits to fully address four more load address commands are needed. This causes I1 pulses to be in sets of five (see Fig. 2).

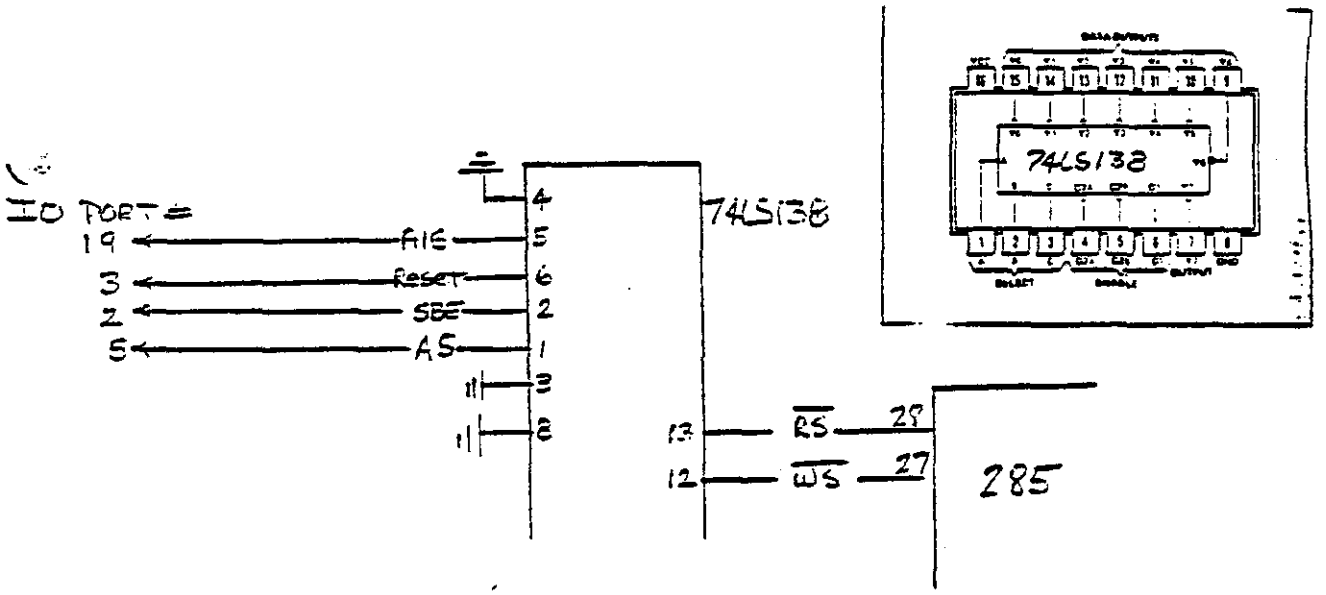
With the address wirtten the next command is a speak. This follows a write-to-speech sequence as previously described. The speak is D1=1, D2=0, D3=1, all other data lines are dont care states. The ready release again is completed when the data has been latched in. The TMC 0285 iwll then issue an IO pulse (Read) to the PHROM and a byte of data will be read in serially through U1-21 (ADD8). The TMC 0285 will continue to send Io pulses as required to supply the data necessary to speak the word until a stop code is encountered. Speech activity will then stop until the next command is written to the speech module. During speech the audio wave form may be observed by looking at U1-18, note that I10 Pin-44 is a low impedence across which little or no A.C. voltage will be observed.

If it unknown to the CPU what the speech module is doing it's status may be read. This is accomplished by issuing a SPEECH READ, address 9400. The TMC 0285 will take the Ready Line low and setup the status on the Data Bus. When the data is stable ready will be released and the status can be read. The status is indicated on Do = Talk status (TS), D1 = Buffer Low (BL), and D2 = Buffer Empty (BE), all active high signals. The BL and BE signals are used when imputting speech data on the Data Bus.

Other commands include READ BYTE used to bring speech data from the PHROMS to the Data Bus, SPEAK EXTERNAL to put speech data into the TMC 0285 via the Data Bus, NOP, RESET, and READ & BRANCH. For further information see the cited documents.



SBE (speech select) initiated by Home Computer CPU starts all activity in the speech synthesizer. This select can be a write to the speech module or a read from the speech module.



A read select (RS) to the 285 is decoded through the LS138 from SBE $\overline{A5}$ $\overline{A15}$ (address 9000). A write select ($\overline{WS}$) is derived from SBE A5 $\overline{A15}$ (adress 9400).

After one of these signals, the 285 will take the system not ready. (Pin 12 of IO will be low).

Original

CLOCK FREQUENCY SET UP

FREQUENCY LIMITS:

BIT RATE = 155 TO 167 KHZ - NOMINAL = 160 KHZ
BIT PERIOD = 6.45 US TO 5.99 US NOMINAL = 6.22 US

SINCE THE 285 INTERNAL OSCILLATOR FREQUENCY VARIES WITH EACH DEVICE, 3 RESISTORS WERE SELECTED SO THAT WHEN 1 OR MORE WERE CUT THE DESIRED RANGE COULD BE SELECTED.

PROCEDURE: POWER UP MODULE AND MEASURE FREQUENCY

1) IF FREQUENCY IS ABOVE 175 KHZ, CUT 1.5 MEG RESISTOR
2) IF FREQUENCY IS 174 KHZ AND BELOW, CUT 3.3 MEG RESISTOR
3) IF NEITHER BRINGS DESIRED RESULTS - TRY CUTTING BOTH

IT HAS BEEN NOTED THAT ON SOME 285 LOTS THESE FREQUENCYS WILL CHANGE.

EXAMPLE:

1) IF FREQUENCY ABOVE 173, CUT 1.5 MEG
2) IF FREQUENCY BELOW 173, CUT 3.3 MEG

ON OCASSION IT MAY BE NECESSARY TO CHANGE THE 270K (R4) TO A 240K AND REPEAT THE ABOVE STEPS.

WHEN ONLY 1 END OF A RESISTOR IS CUT, THE FREQUENCY WILL READ APPROXIMATELY 2 KHZ LOWER THAN WHEN IT IS CUT OUT COMPLETELY.

WHEN CLIPPING RESISTORS, IT IS PERMISSIBLE TO RE-SOLDER ON END INSTEAD OF REPLACING A RESISTOR.

NOTE: AN UNWASHED PCB, LARGE AMOUNTS OF FLUX AROUND OSCILLATOR CIRCUIT, OR CONTAMINATED SOLDER WILL AFFECT FREQUENCY.

SPEECH MODULE TROUBLESHOOTING GUIDE

BLACK SCREEN UPON POWER-UP

1. Check for -5 to +5 short on 350 stack. (Pins 1 and 2). Since +5 goes to other pins it may appear to be shorted elsewhere, but it is usually the 2325 shorted internally.

2. If unit has shields check connector pins 1 (+5) and/or 43 (-5) to shield (ground). If shield is shorted to either, remove shields and measure again. If not shorted with shields off, check for short between R4, 5, 6, 7 and etch directly above; or 285 or 350 substrate may be touching shield.

3. Shorts on flex cable.

4. Check for clock.

5. Short on 44 pin connector.

6. Open lead (pin) on 44 pin connector.

7. Short on or shorted .1uf caps (C4, C5).

LOCK UP AFTER ENTERING WORD/S

1. Check 3904 transistor to make sure it is in correctly, broken lead, defective.

2. Check for clock at both 285 and stack.

3. Check address lines for signals when unit in idle mode. If signal present (some sort of waveform) and pin is not shorted to another line, 285 is defective. Note: All other signals may be garbage and ready may stay high.

4. Check IO and I1 (control lines) these allow idle, load-address, and read functions to occur. Hit shift Q and monitor lines. If they stay low - 285 defective.

5. Check data lines. If signal missing, probably one line shorted to another.

6. Check LS138 and see if SBE present (pin 2).

7. Check RS and WS at 285 (pins 28 and 27). If both low (active) at same time check for shorted lines. These lines may be incorrect however, depending on other signals.

8. Check for flux conducting on PCB around MOS or flex cable.

9. Cold solder on 350 stack.

10. Other shorts at practically any location.

11. Defective 350 stack. similiar to defective 285; however, in some cases I0 and I1 taking a fairly long time to change states (even though unit locked up) indicate adefective stack.

12. Defective 285. In some cases address lines, data lines etc., will be ok - but ready (pin 18 on 285) will go high and stay there.

Garbled on tester - Sounds ok on computer. 285 defective. Tester checks at different voltage levels, so this may indicate 285 out of voltage box spec.

Speaks on tester - Won't on computer. 285 defective, opens, shorts on connector.

Speak external (call spget) only - Defective. 285 defective.

No clock. 285 defective, shorts in oscillator circuit (R4, 5, 6).

FREQUENCY WON'T ADJUST

1. Cold solder on R4, 5, 6 - or broken etch.

2. Flux conducting anywhere near the above parts.

3. Wrong value resistors, solder shorts.

   Note: Rarely you may find a 285 where the clock frequency, will not adjust by removing one or both resistors. In this case you may have to change R4 to a 240K and repeat normal steps. 285 is usable - do not scrap!

Won't speak or level low. R3 wrong value, C2 defective, short on (pin 8-285). Defective 285.

NO VOCABULARY PLUGGED IN - APPEARS ON SCREEN

1. Cold solder on stack.

2. 2325 defective.

3. LS138 defective (very rare).

4. 285 defective.

5. Solder shorts.

6. 3904 transistor bad.

7. No clock at stack.

FUNCTIONAL TESTER READOUTS AND OR OTHER FAILURES

1. Phrom-0 2325 or almost any short.

2. Phrom-1 2326

3. Command reset-285

4. Power up-3904XSTR, shorts, 138, clock,* 285, shorts on connector.

   Note: A defective 3904 can effect ready turn around timing and thus fail for power up. Since the 285 has it's own internal power-up clear circuitry; however, the 285 could possibly cause this condition also. * shorts on 285 and 350.

5. Speech garbles only on tester. Defective 285.

6. Speak EXT. a) wrong values. b) 285.

Fails EPROM (EPROM command module) only. Shorts on 285, stack, connector.

   Note: Any continuous failures on functional tester usually indicate dirty contacts on tester board.

Light won't come on on PHROM tester. Edge contacts dirty on speech PCB.

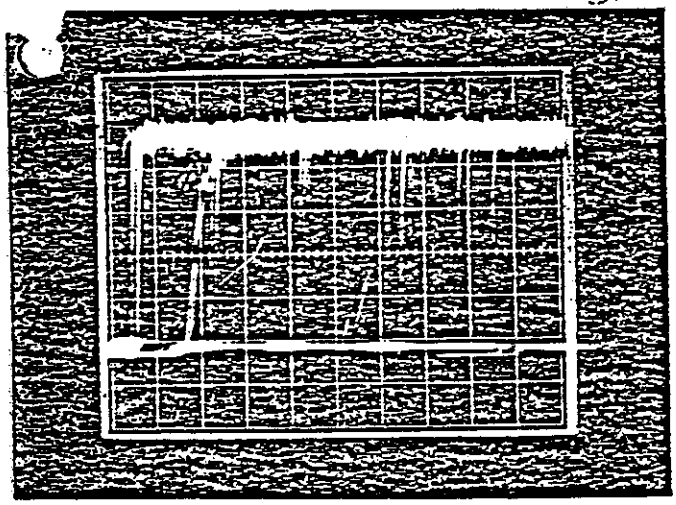
3060 Failures. (See readout sheet). Shorts are probably accurate. Opens are usually dirty contacts on speec PCB.

Won't work in case. Shield short to etch in front of 350 stack. 285 or 350 substrate short to shield. Any +5 or =5 short to ground, cold or insufficient solder on 44 pin connector.

Frequency won't adjust on test set. As before, plus insufficient solder on PCB - interconnect.

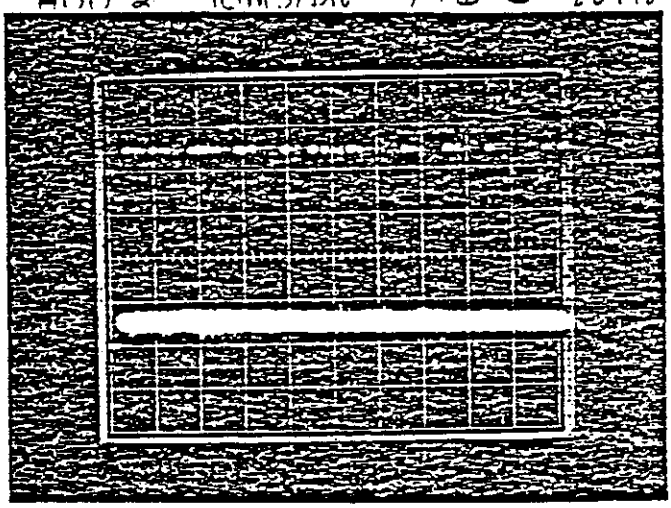
   Note: This is intended as a basic guide and generally applies to uits that have passed shorts and open tests. At PCB level only, assume shorts before components. For complete 285 theory see drawing number 1501640.

10 MS/DIV

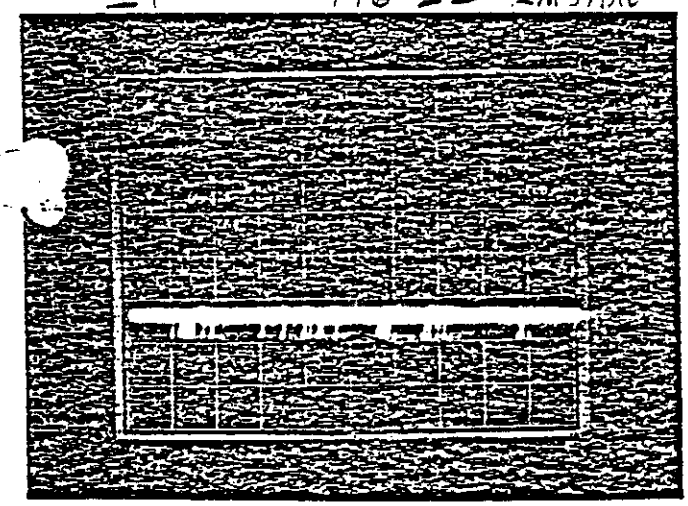


ready

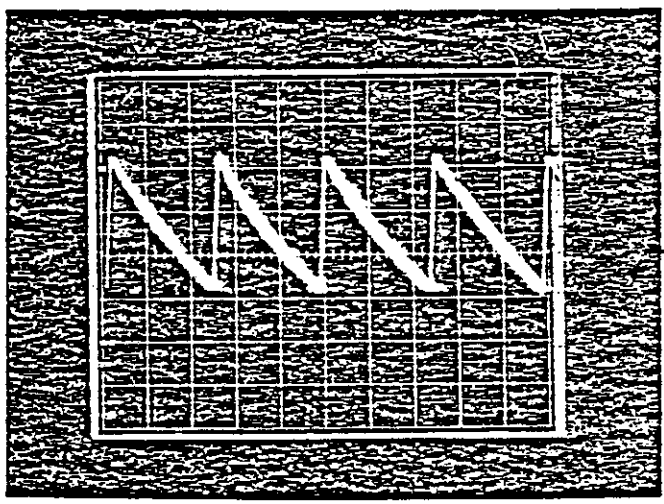
ADD 2 10MS/DIV FIG 3 2V DIV



I1 FIG #2 2V/DIV 2MS/DIV

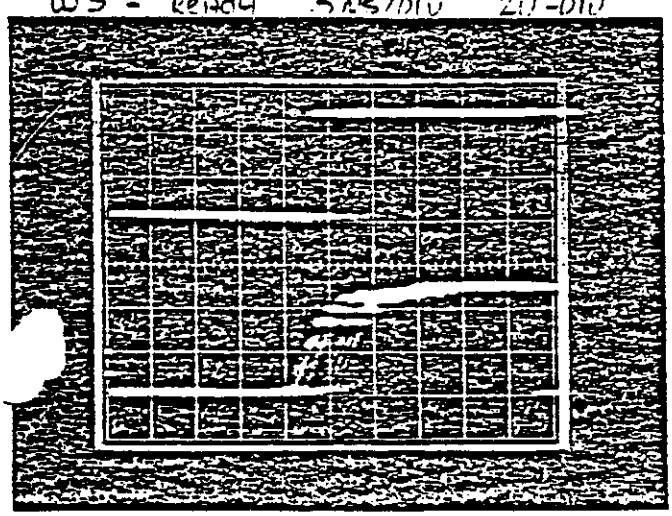


OSC



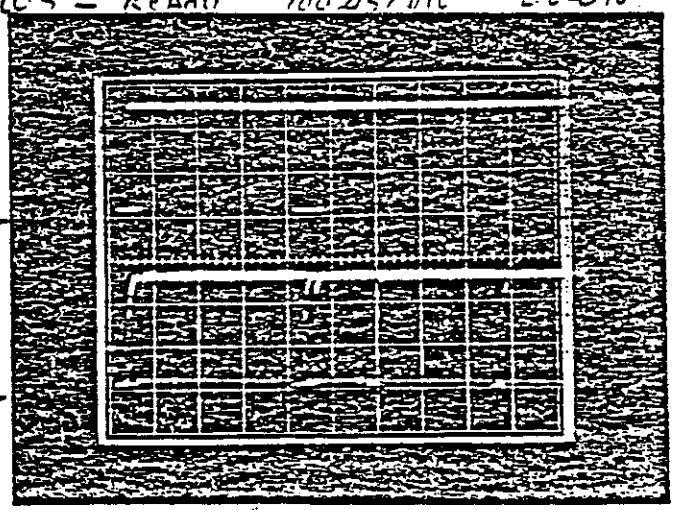
1V/DIV 1MS/DIV

WS - Ready 5MS/DIV 2V-DIV

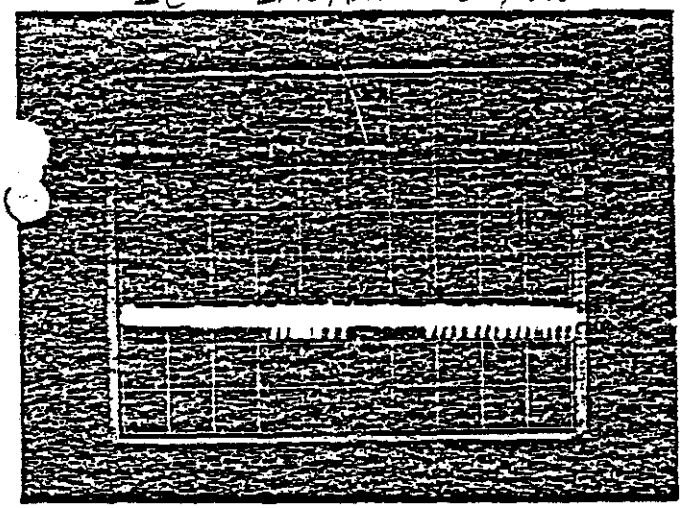


CALL SAY 'LOOP'

WS - Ready 100 US/DIV 2V-DIV



CALL SAY 'LOOP'


LO
2MS/DIV
2V/DIV

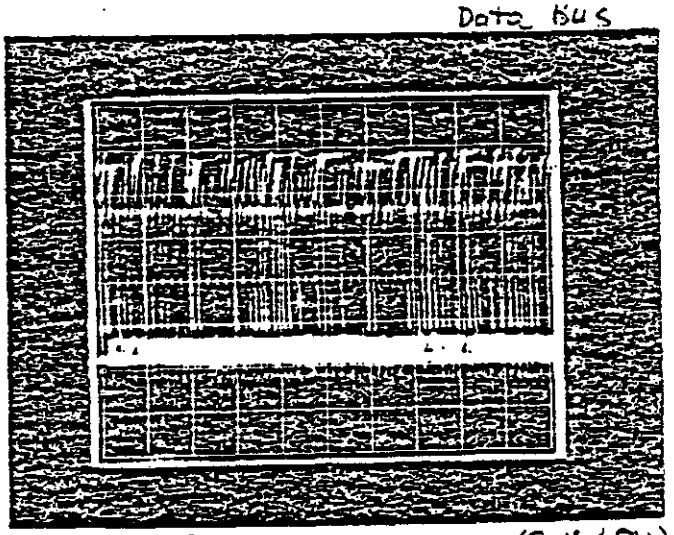
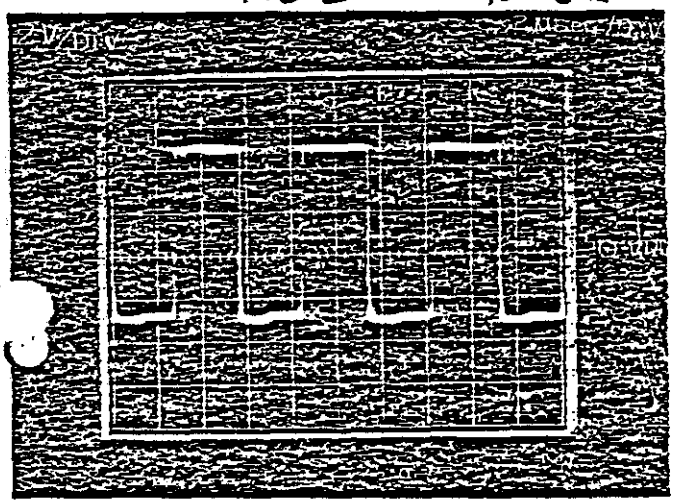
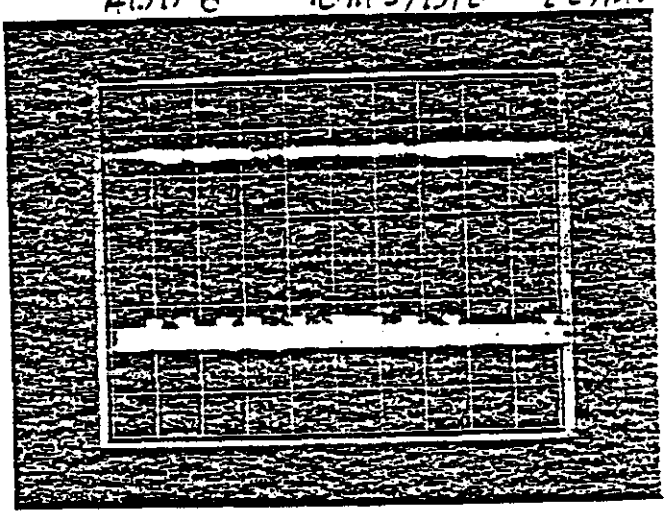

Data Bus
1V/DIV
10MS/DIV

FIG 1 Rom CIK


2V/DIV


ADD 8
10MS/DIV
2V/DIV

Peripheral I/O S&O Test (3060)

The output side (J2) of the peripheral has the same number configuration as the 3060. (1 thru 44)
1, 2, 43, 44 NOT used

The input side (J1) is configured as follows:

3060 #	J1 #	3060 #	J1 #
45	1	75	31
46	2	76	32
47	3	77	33
48	4	78	34
49	5	79	35
50	6	80	36
51	7	81	37
52	8	82	38
53	9	83	39
54	10	84	40
55	11	85	41
56	12	86	42
57	13	87	43
58	14	88	44
59	15		
60	16		
61	17		
62	18		
63	19		
64	20		
65	21		
66	22		
67	23		
68	24		
69	25		
70	26		
71	27		
72	28		
73	29		
74	30		

INPUT side

PINS 2-42 ARE 45 TO 87 "TO" 3060

" 1-43 ARE 46 TO 88 "TO" 3060

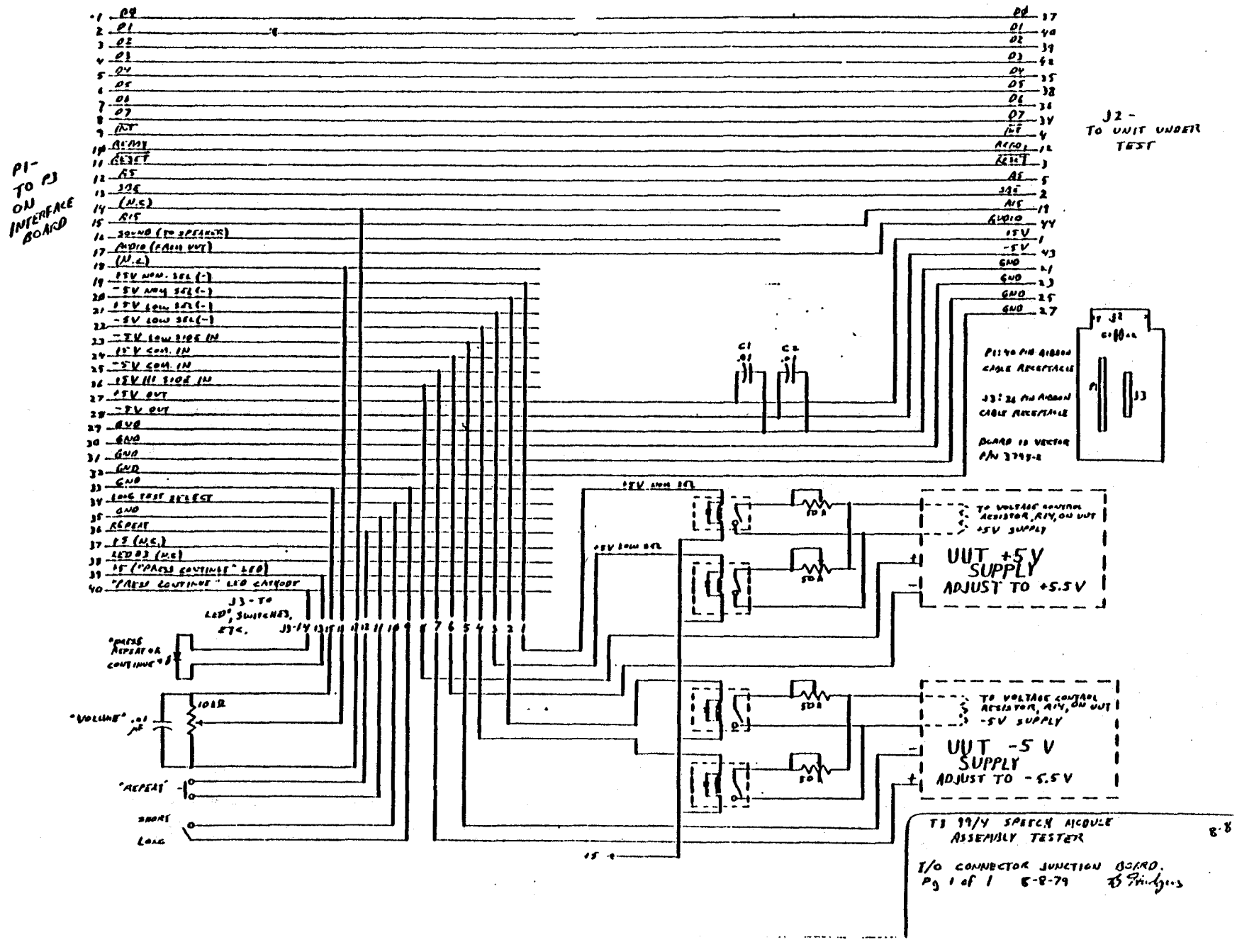
SPEECH I/O CONTINUITY TEST FIXTURE
PERIPHERAL I/O CONTINUITY TEST FIXTURE

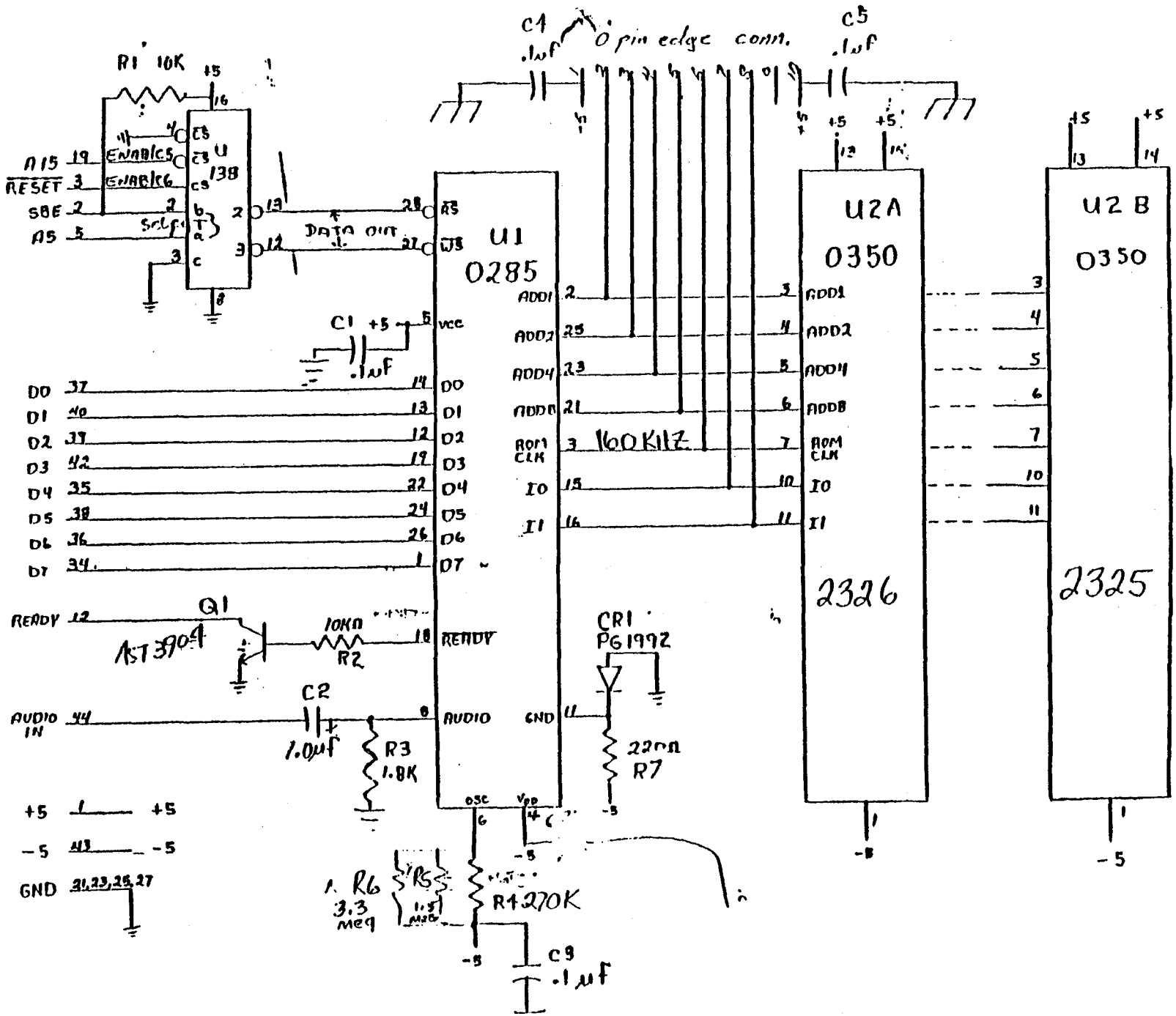
These fixtures will test all the peripherals in OR out of the plastics. (the speech module is tested on a seperate fixture) The test checks for shorts and opens between the I/O ports only.

As an aid for troubleshooting the node numbers and their corresponding peripheral pin numbers are listed as follows:

INPUT SIDE P1		OUTPUT SIDE P2	
node#	periph#	node#	periph#
1	1	45	1
2	2	46	2
3	3	47	3
4	4	48	4
5	5	49	5
6	6	50	6
7	7	51	7
8	8	52	8
9	9	53	9
10	10	54	10
11	11	55	11
12	12	56	12
13	13	57	13
14	14	58	14
15	15	59	15
16	16	60	16
17	17	61	17
18	18	62	18
19	19	63	19
20	20	64	20
21	21	65	21
22	22	66	22
23	23	67	23
24	24	68	24
25	25	69	25
26	26	70	26
27	27	71	27
28	28	72	28
29	29	73	29
30	30	74	30
31	31	75	31
32	32	76	32
33	33	77	33
34	34	78	34
35	35	79	35
36	36	80	36
37	37	81	37
38	38	82	38
39	39	83	39
40	40	84	40
41	41	85	41
42	42	86	42
43	43	87	43
44	44	88	44

NOTE: This document supersedes any ones previous to 05/05/80


P1- TO PJ ON INTERFACE BOARD
J2 - TO UNIT UNDER TEST
P0
P1
P2
P3
P4
P5
P6
P7
INT
READY
RESET
RS
WE
(N.C.)
MIE
SOUND (TO SPEAKER)
AUDIO (FROM UUT)
(N.C.)
+5V NOM. SEL (-)
-5V NOM. SEL (-)
+5V LOW SEL (-)
-5V LOW SEL (-)
-5V LOW SIDE IN
+5V COM. IN
-5V COM. IN
+5V HI SIDE IN
+5V OUT
-5V OUT
GND
GND
GND
GND
LONG TEST SELECT
GND
REPEAT
P5 (N.C.)
LED B3 (N.C.)
P5 ("PRESS CONTINUE" LED)
"PRESS CONTINUE" LED CATHODE
J3 - TO LED's, SWITCHES, ETC.
J3-24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1
C1
C2
P1 TO PIN RIBBON CABLE RECEPTACLE
J3: 24 PIN RIBBON CABLE RECEPTACLE
BOARD IS VECTOR P/N 3795-2
+5V NOM SEL
+5V LOW SEL
TO VOLTAGE CONTROL RESISTOR, R1V, ON UUT +5V SUPPLY
UUT +5V SUPPLY ADJUST TO +5.5V
TO VOLTAGE CONTROL RESISTOR, R1V, ON UUT -5V SUPPLY
UUT -5V SUPPLY ADJUST TO -5.5V
"PRESS REPEAT OR CONTINUE" SW
"VOLUME" .01 μF
10KΩ
"REPEAT"
SHORT
LONG
+5 V
TI 99/4 SPEECH MODULE ASSEMBLY TESTER
I/O CONNECTOR JUNCTION BOARD.
Pg 1 of 1 8-8-79 BS Shirley
8-8


R1 10K
+5
A15
RESET
SBE
A5
ENABLE5
ENABLE6
Sel
U 138
DATA OUT
U1
0285
C1 .1uF
C1
.1uF
40 pin edge conn.
C5
.1uF
U2A
0350
2326
U2B
0350
2325
160KHZ
D0
D1
D2
D3
D4
D5
D6
D7
READY
Q1
2N3904
10KΩ
R2
CR1
PG1992
AUDIO IN
C2
1.0uF
R3
1.8K
220Ω
R7
+5
-5
GND
R6
3.3 meg
R5
R4 270K
C9
.1uF