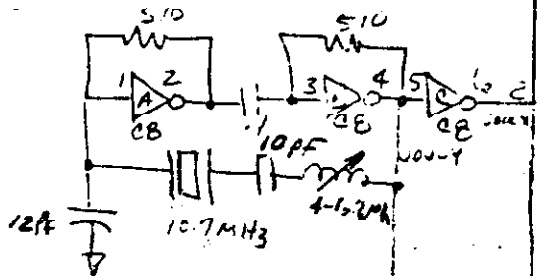
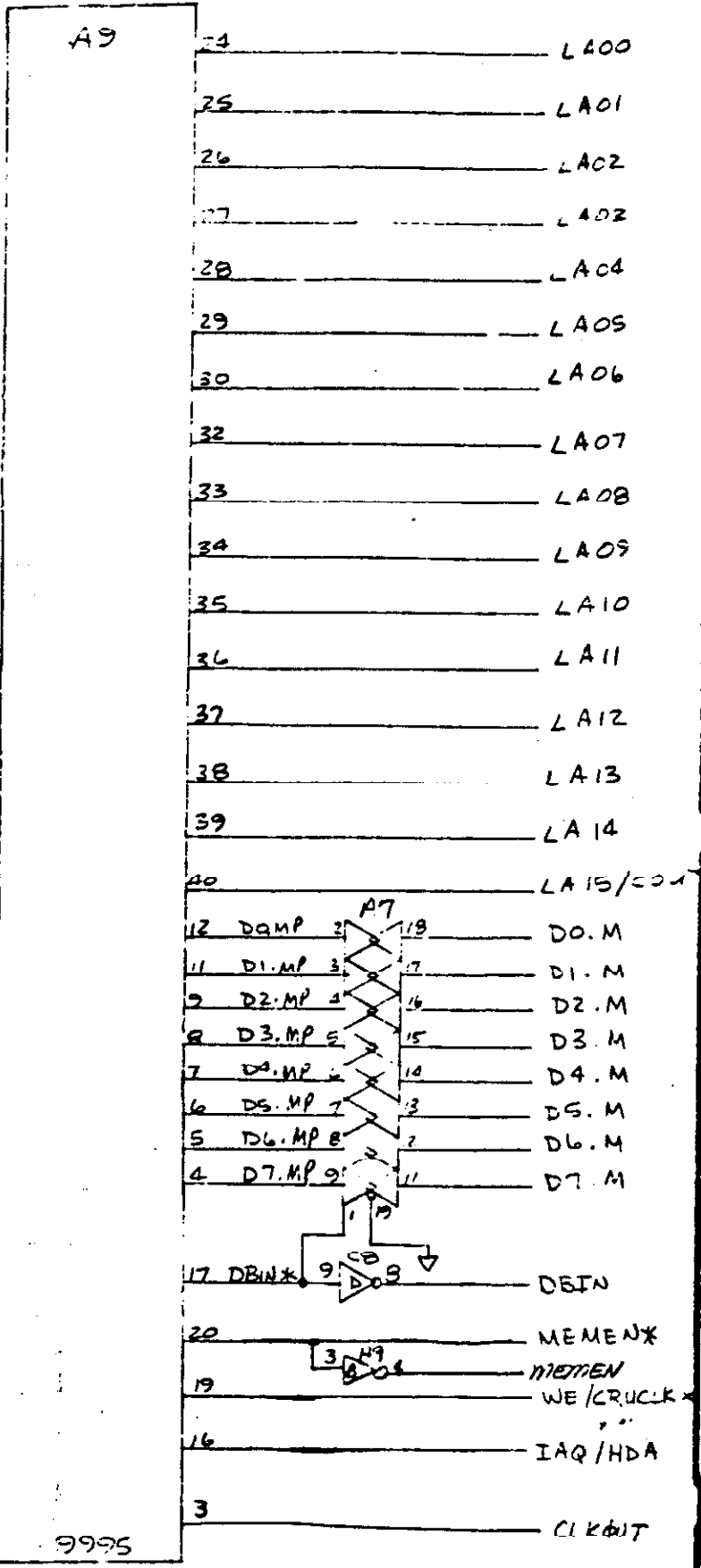
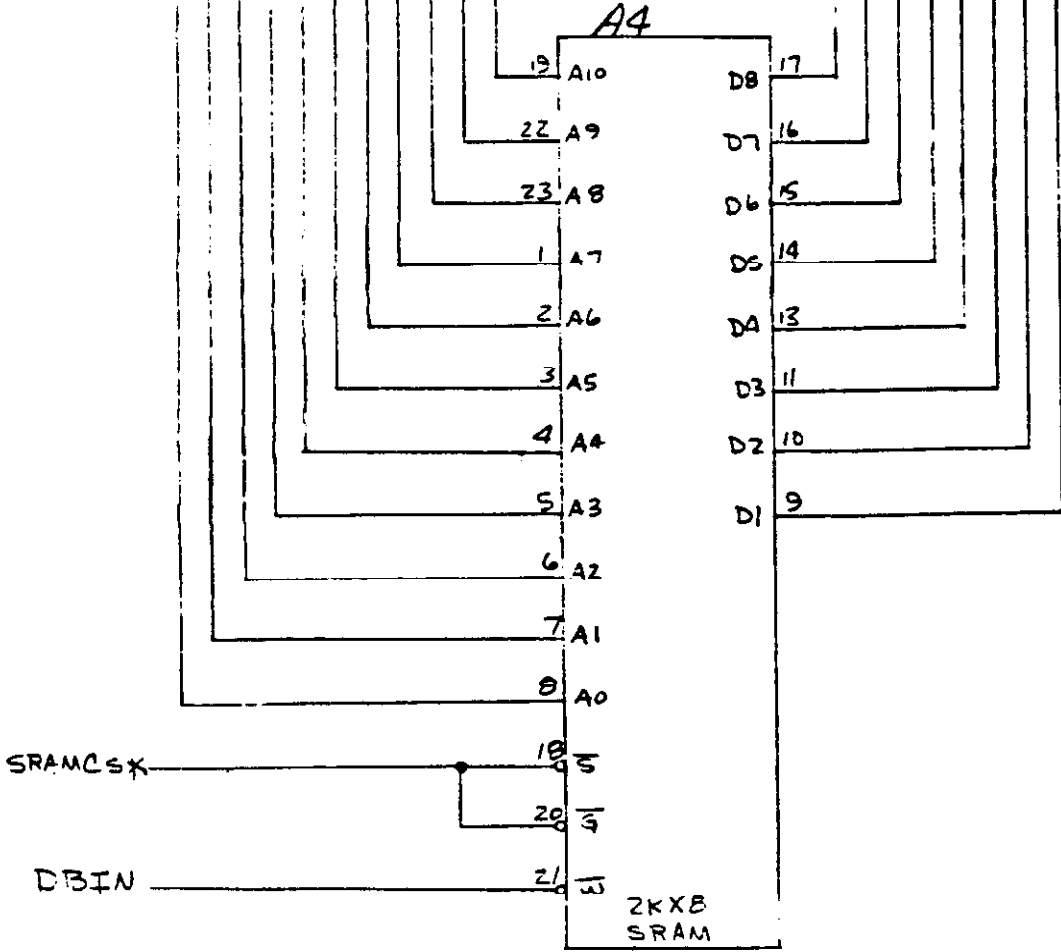
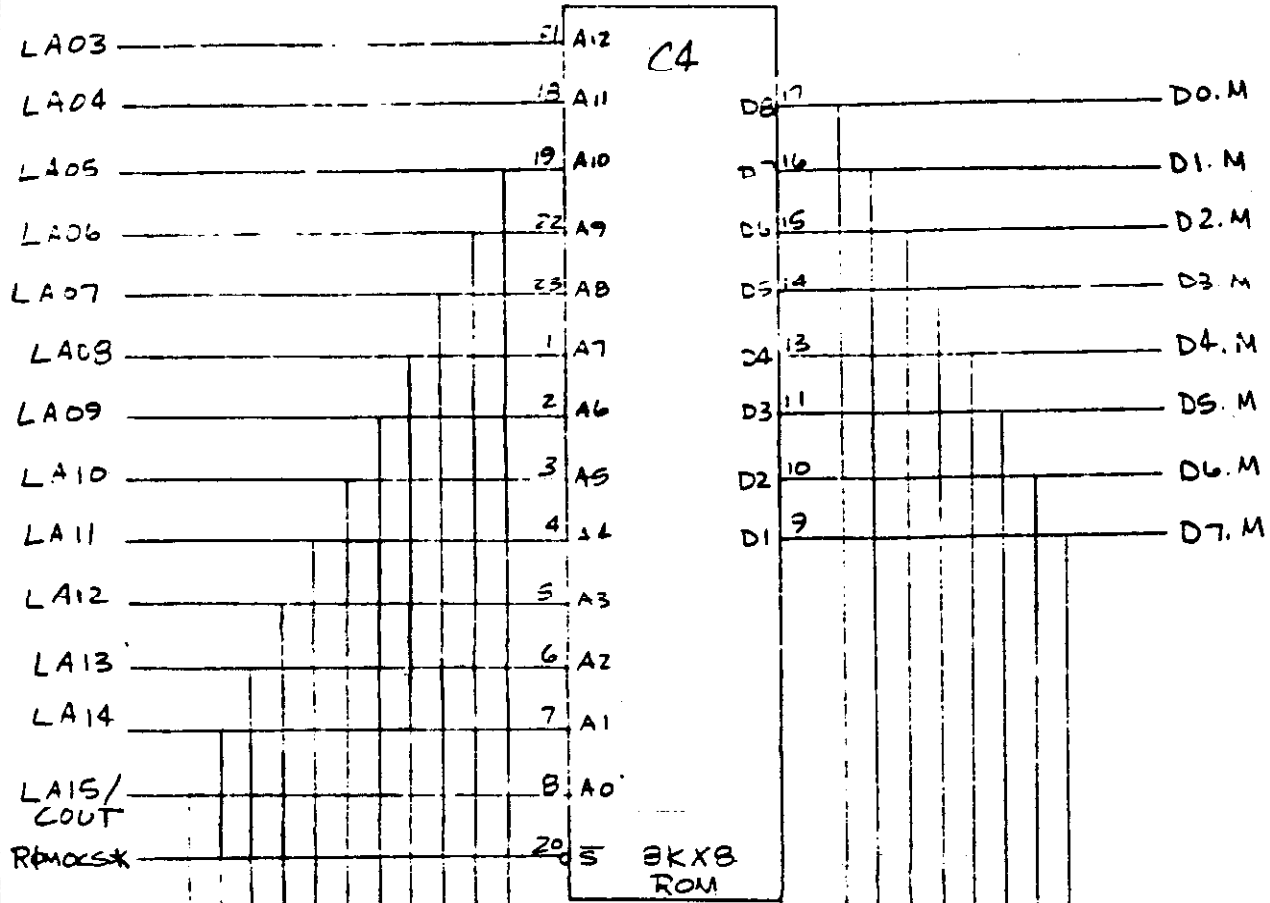


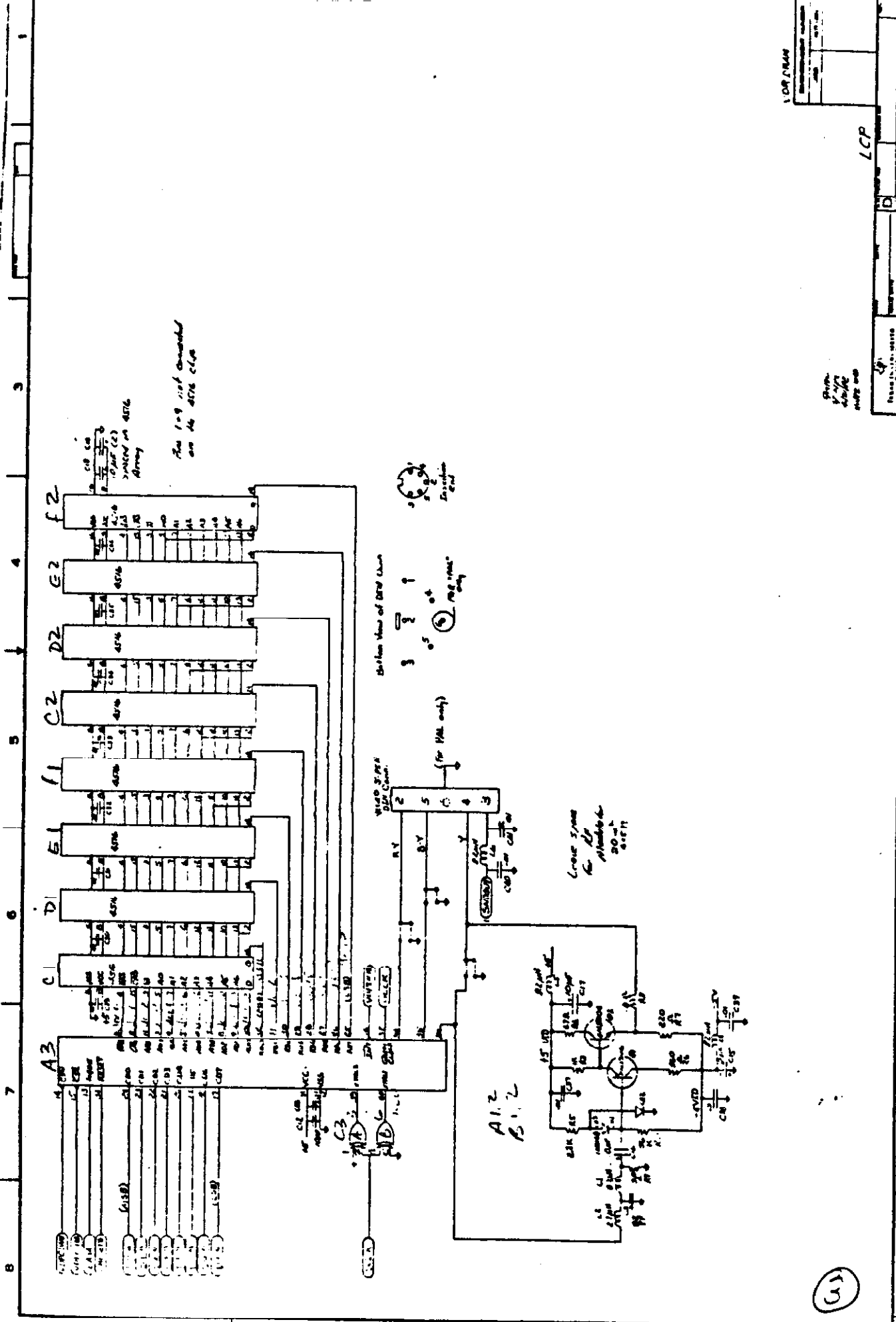
1/25/35



SCLK

①



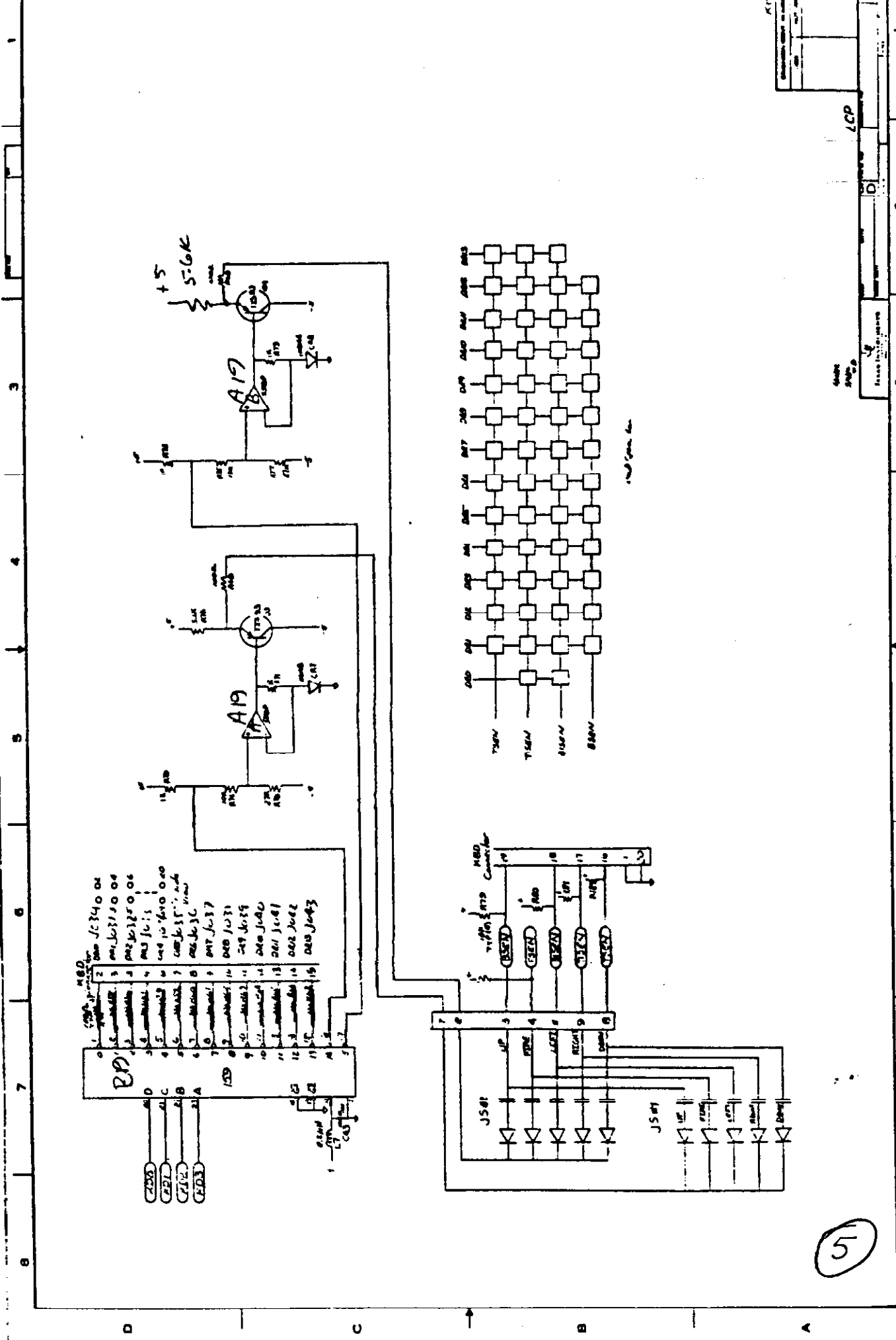


1 OF 2 PAGES
LCP

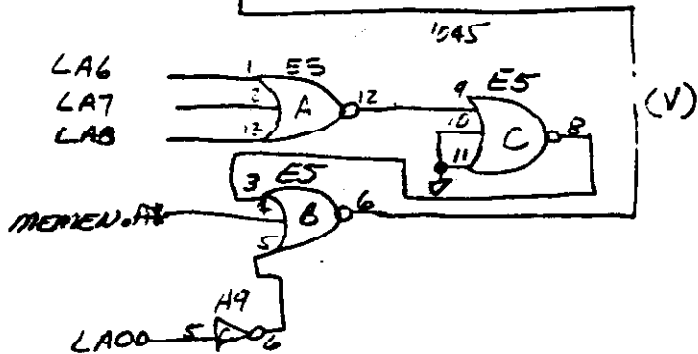
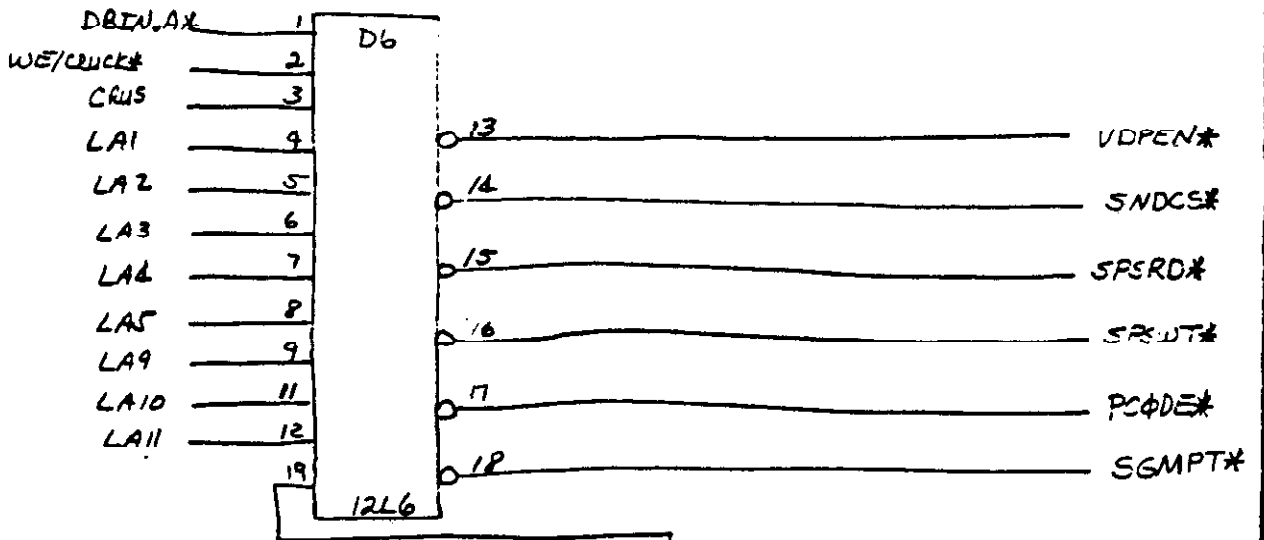
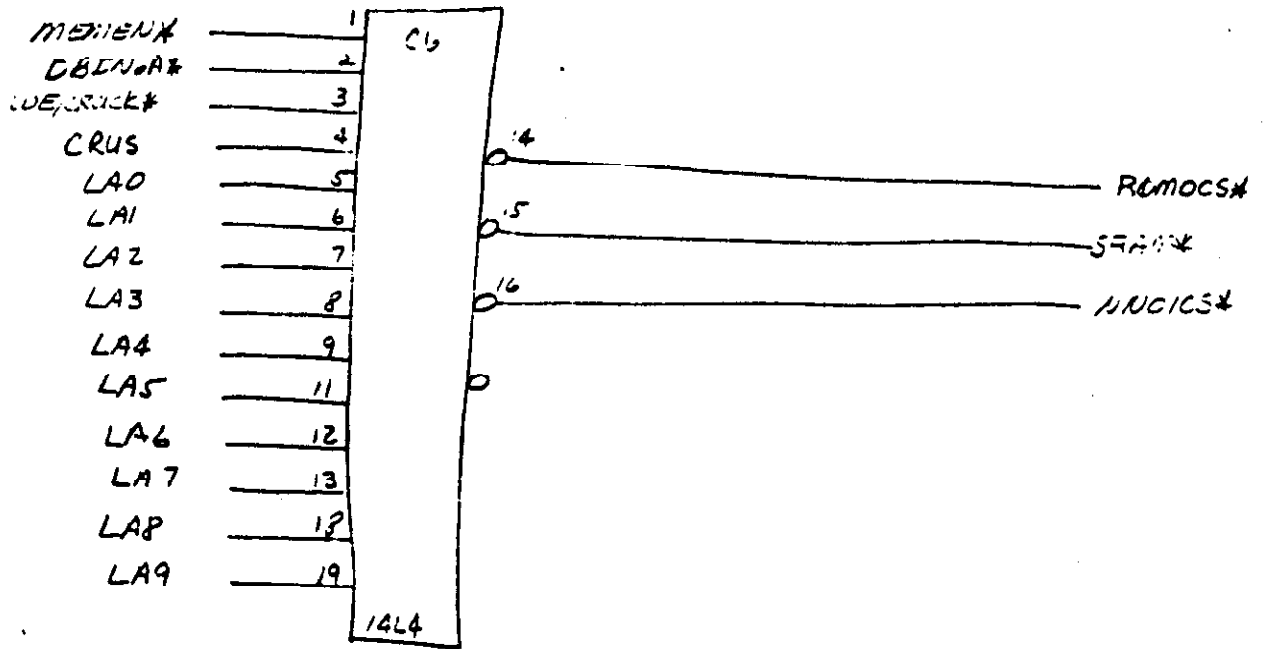
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of
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Part
of
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4576
4576

51

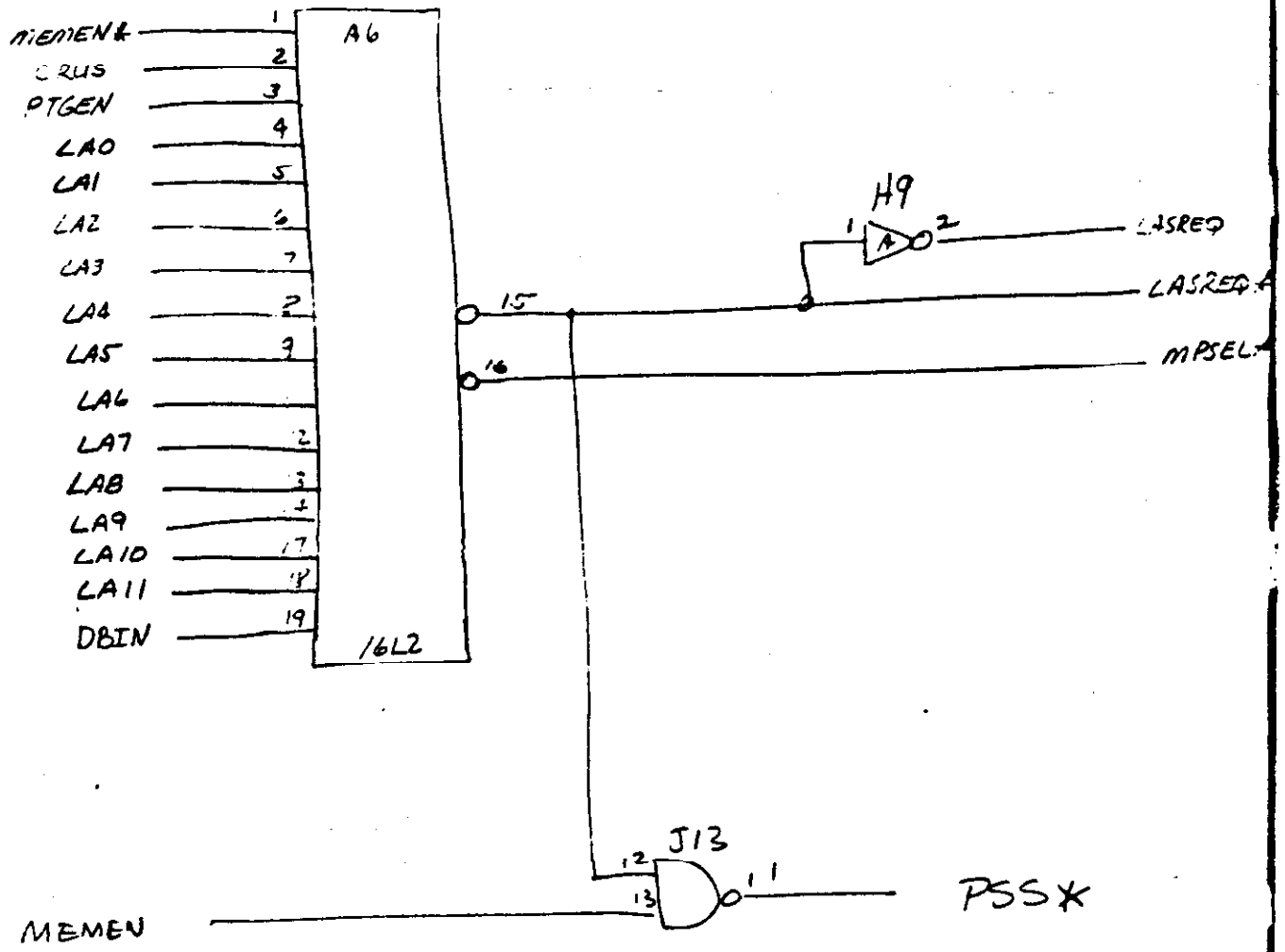


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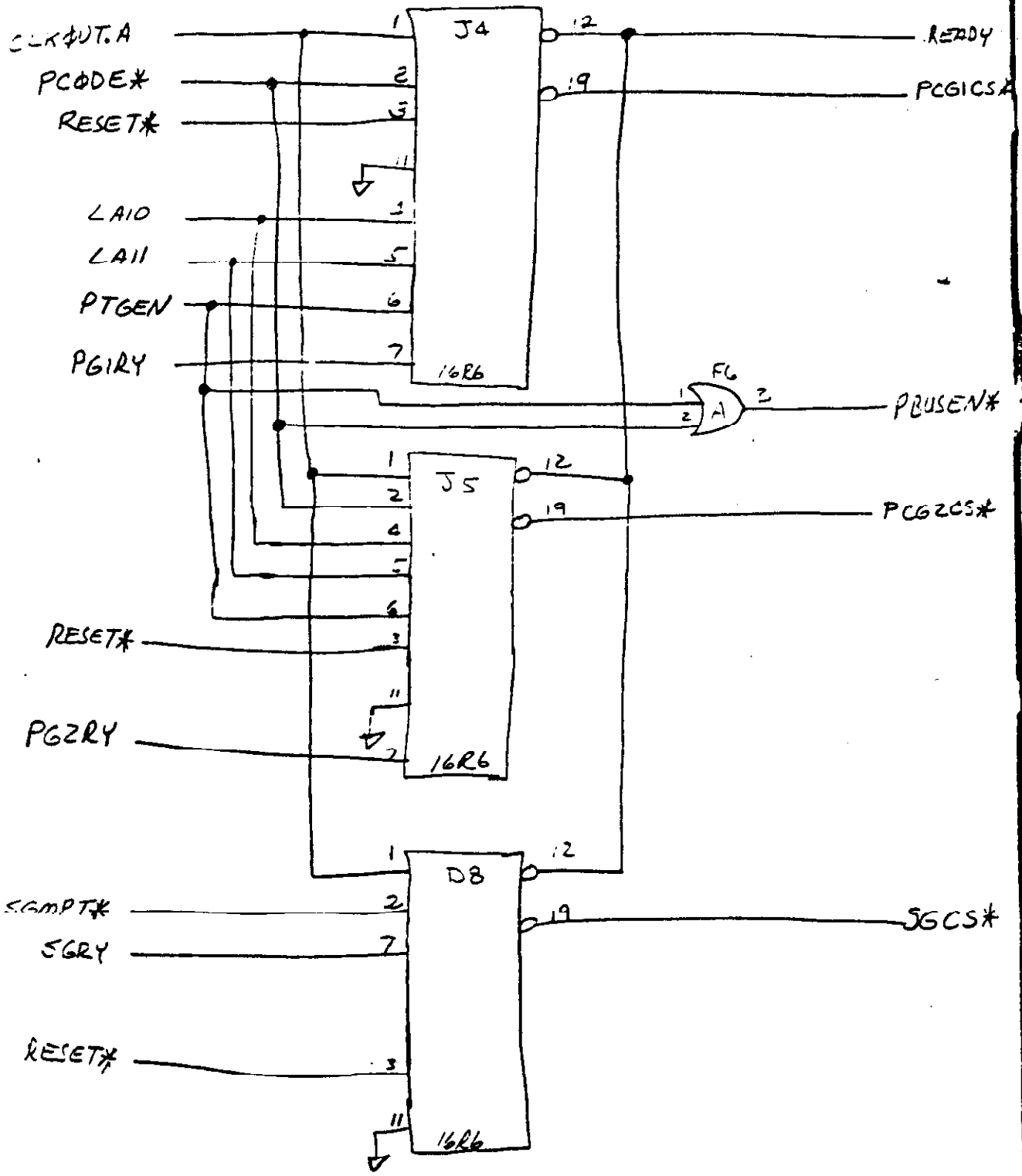


LAS Decode PIA's

(6)

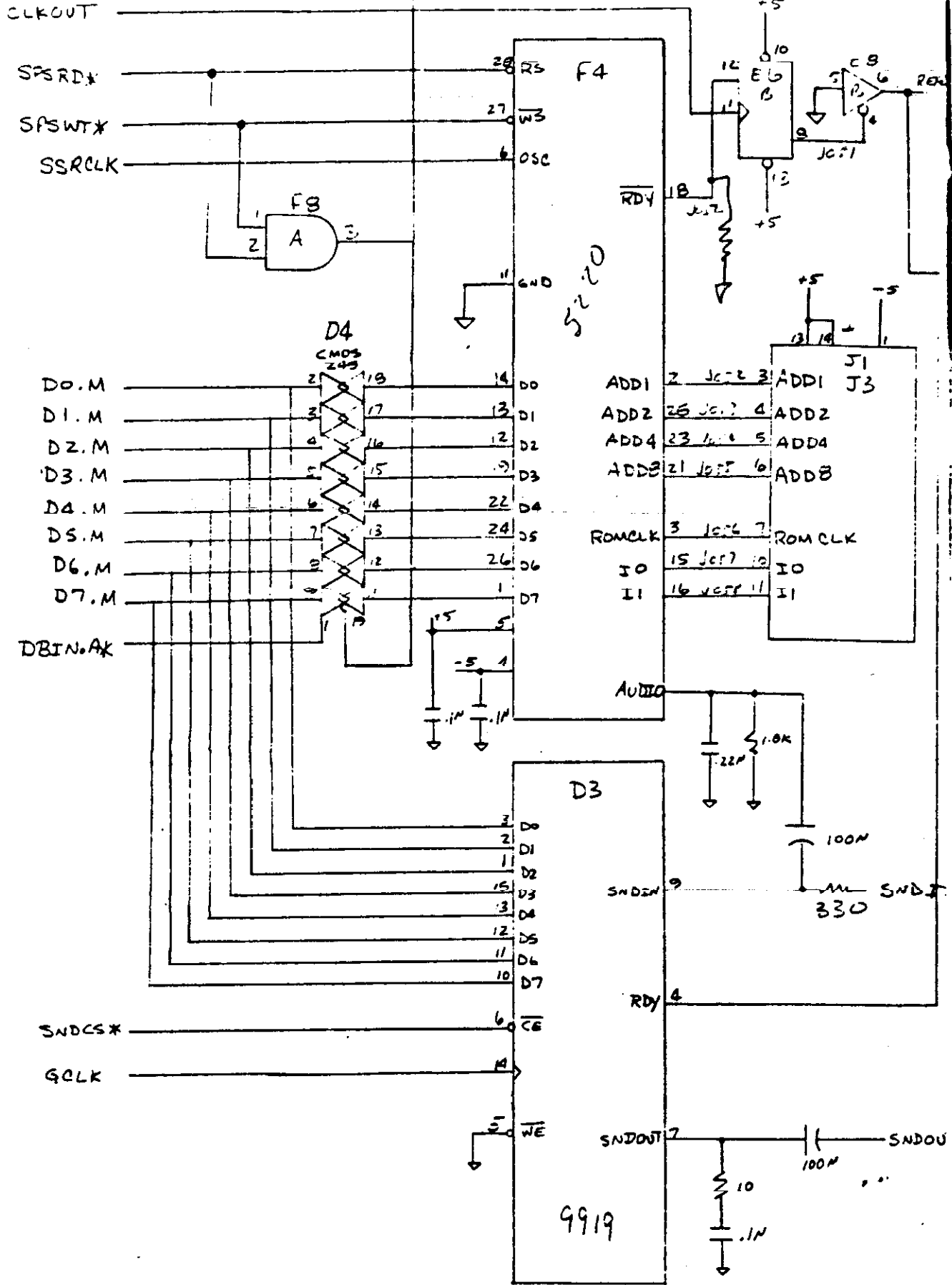


Selects for 1/5. MAPA PLD

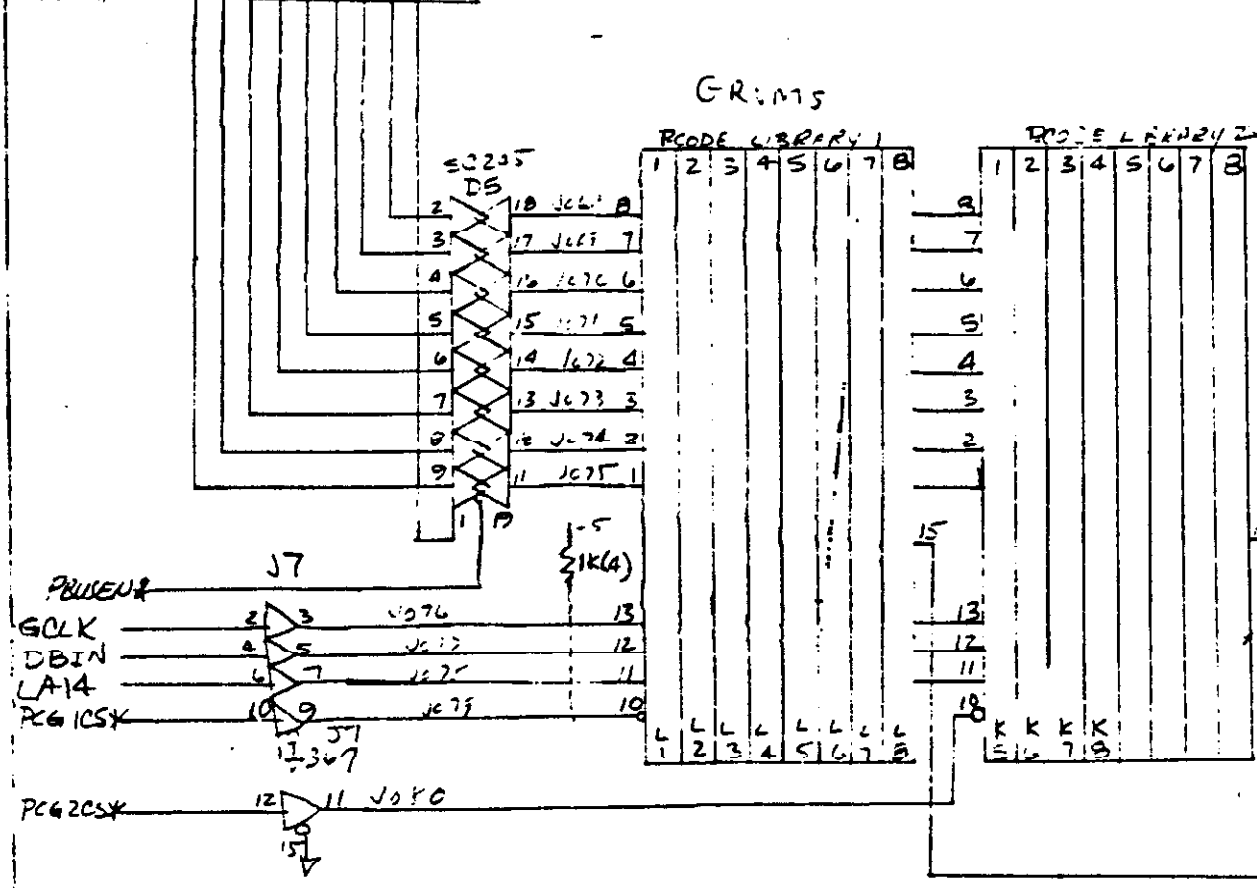
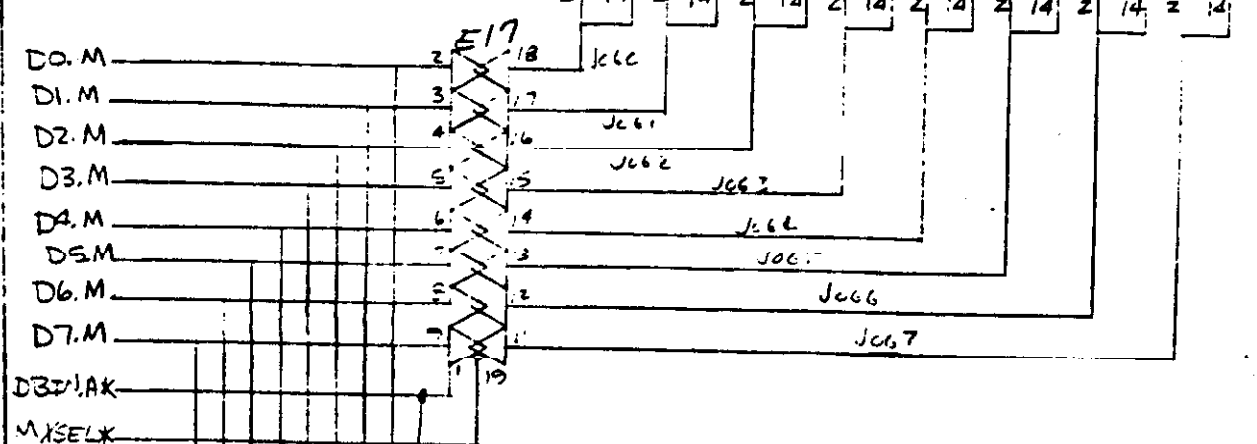
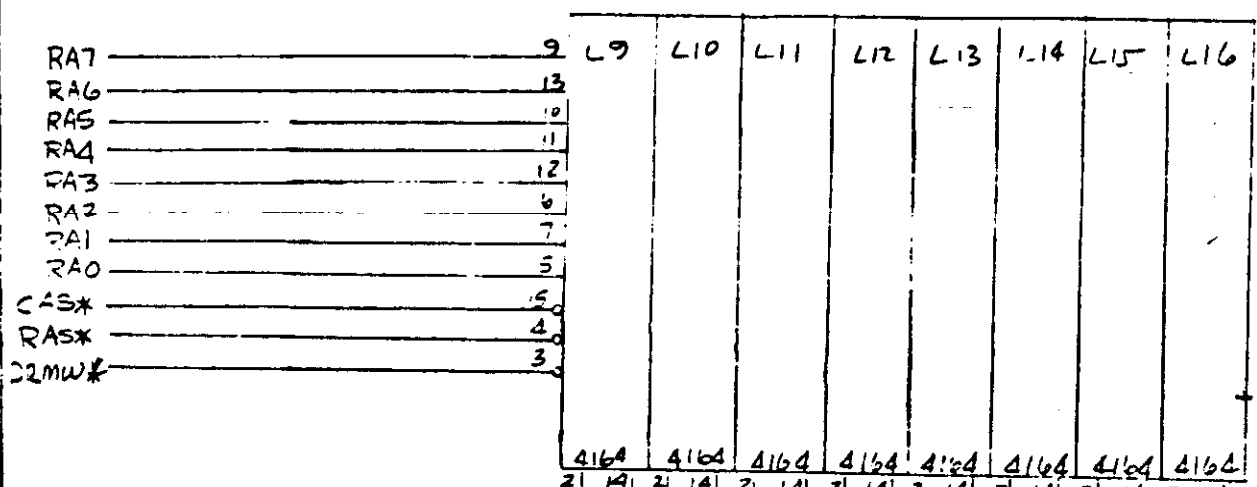


GROM Protect Logic

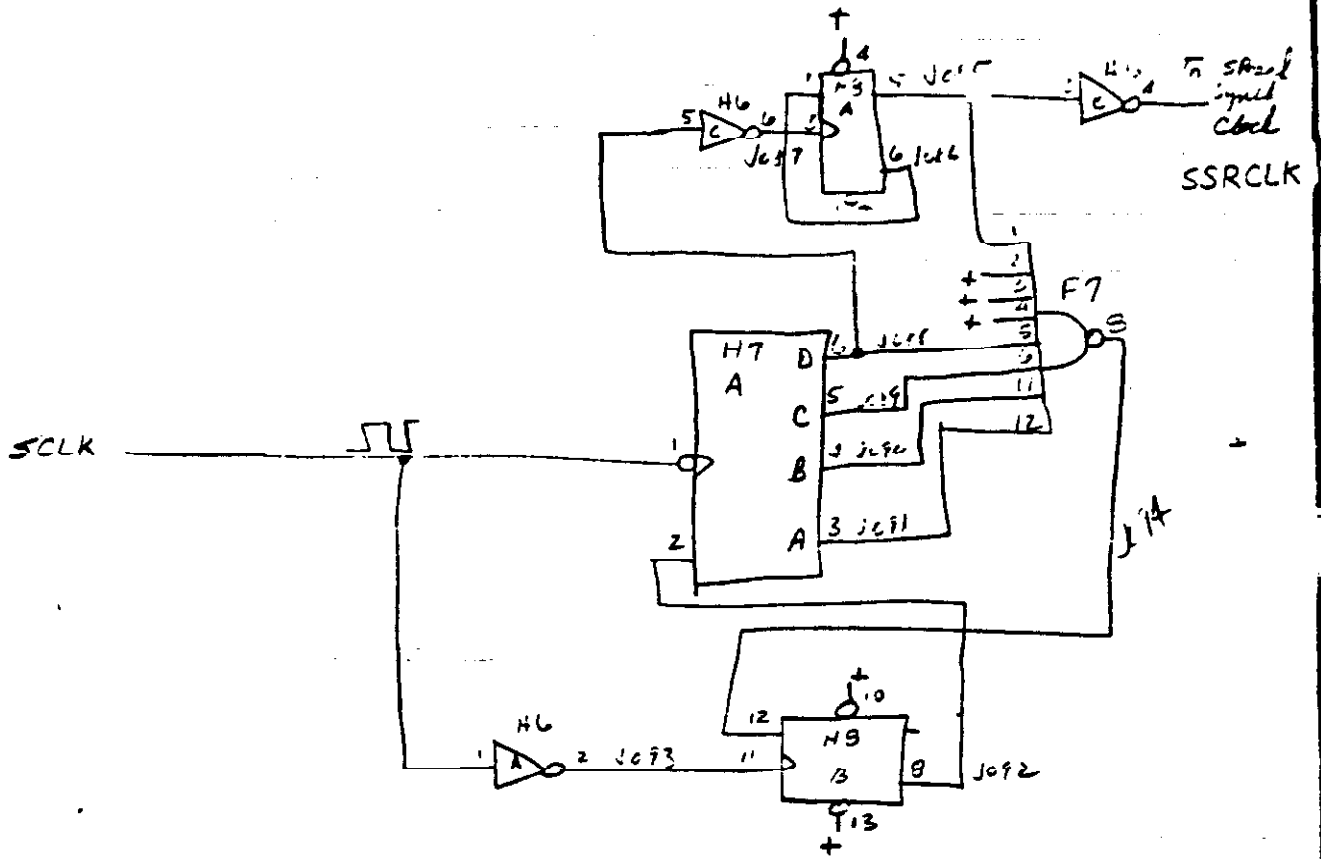




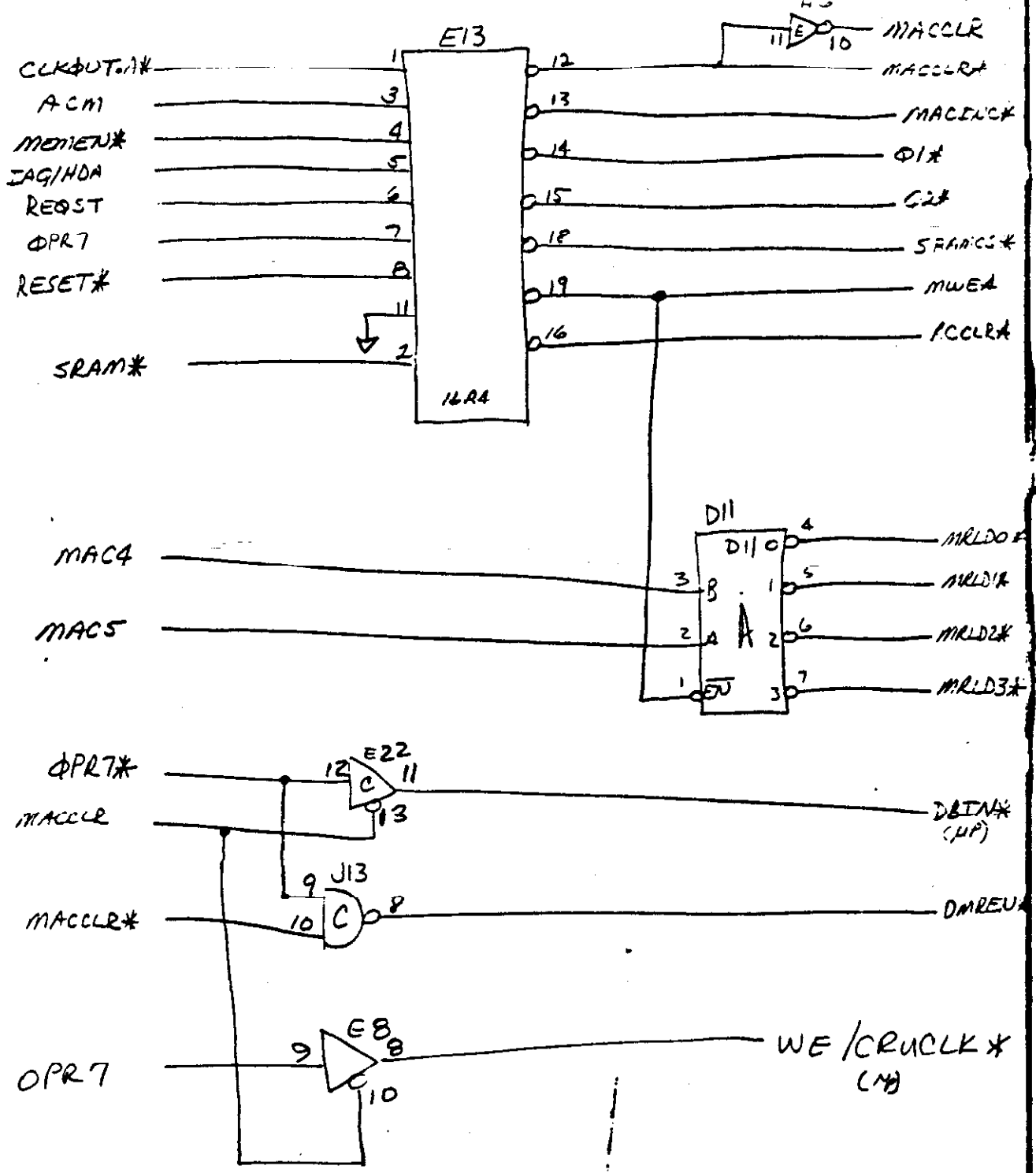
Speech, Sound Gen



DRAM PCODE LIBRARIES

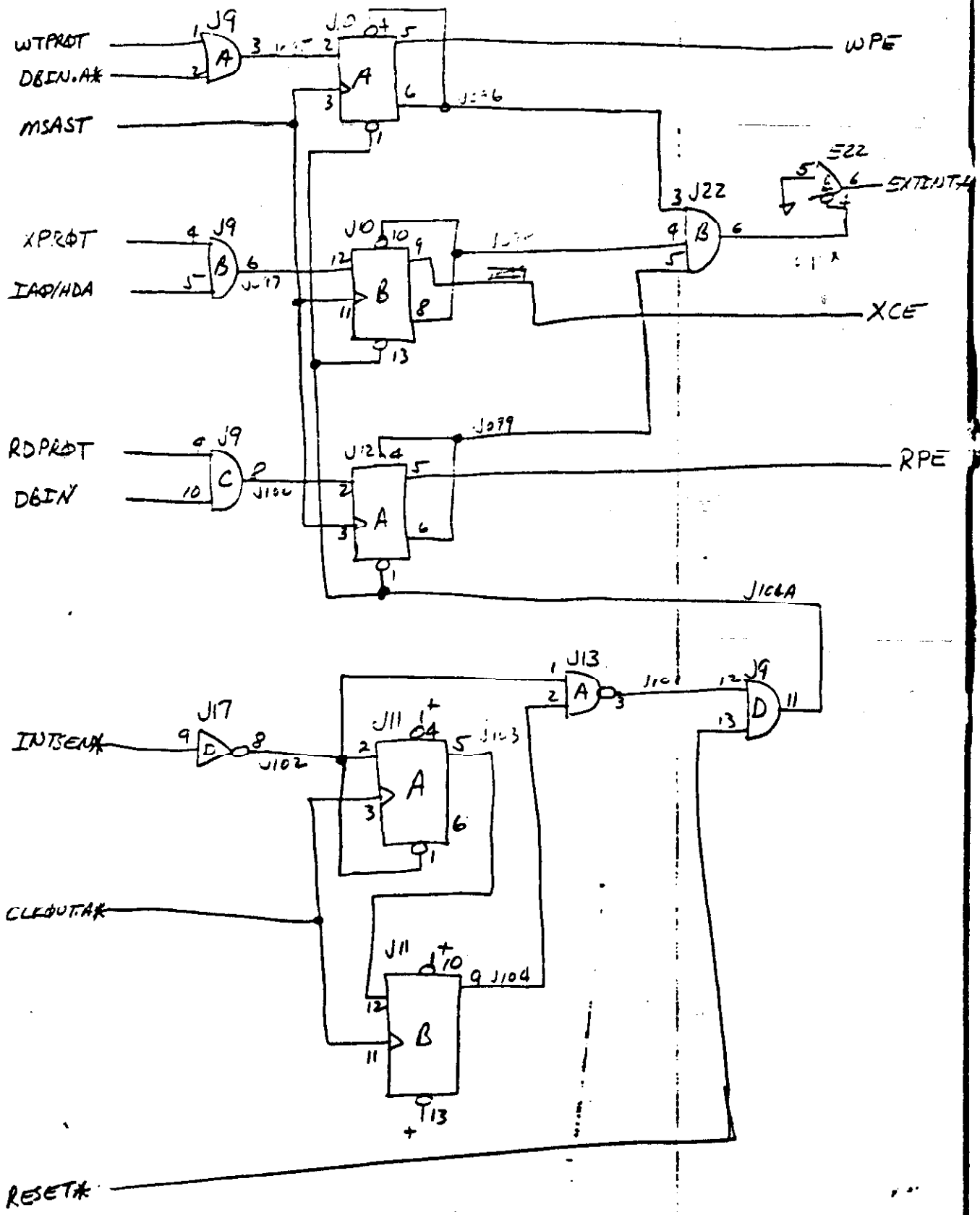


Speed Signal. Clock

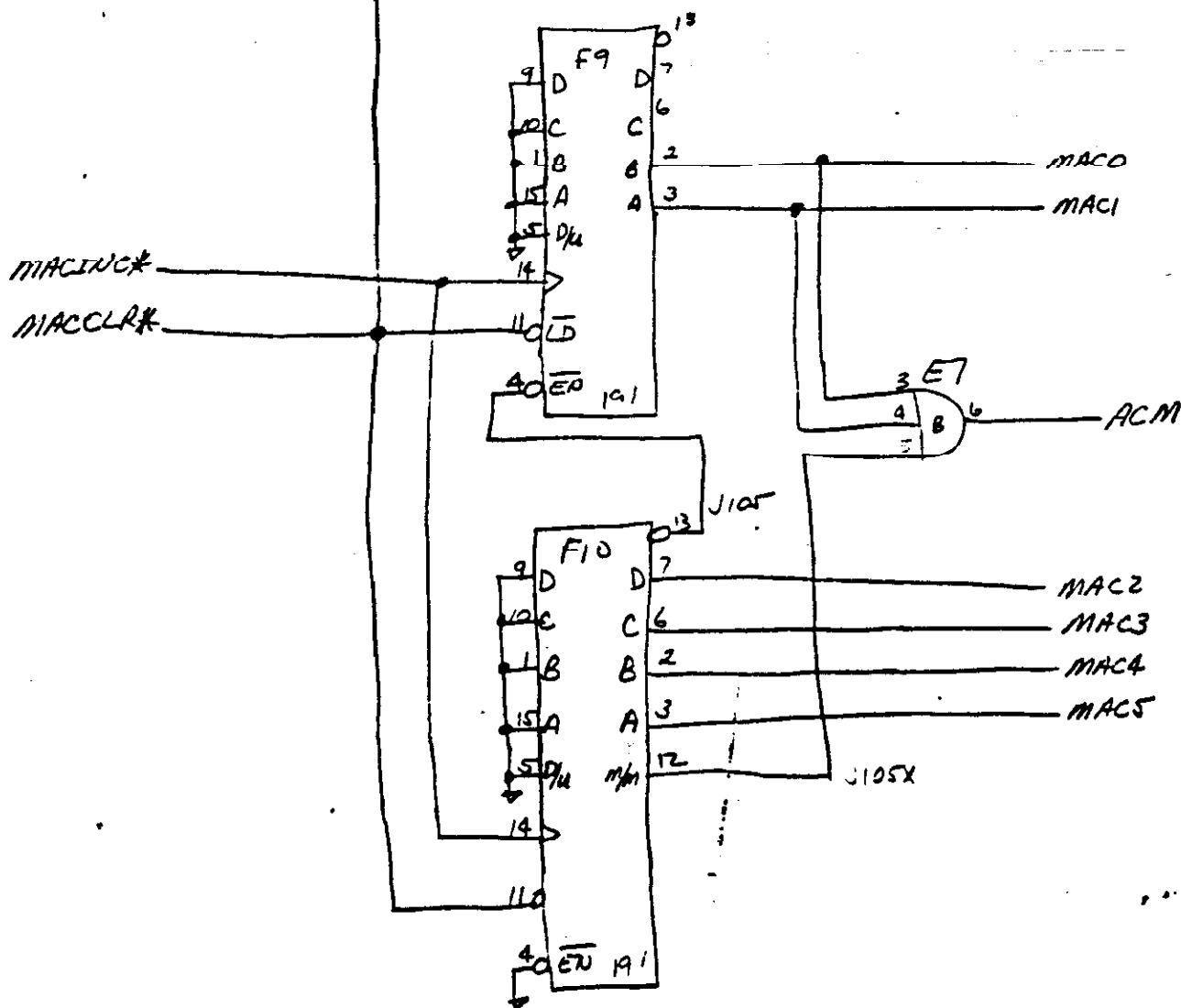
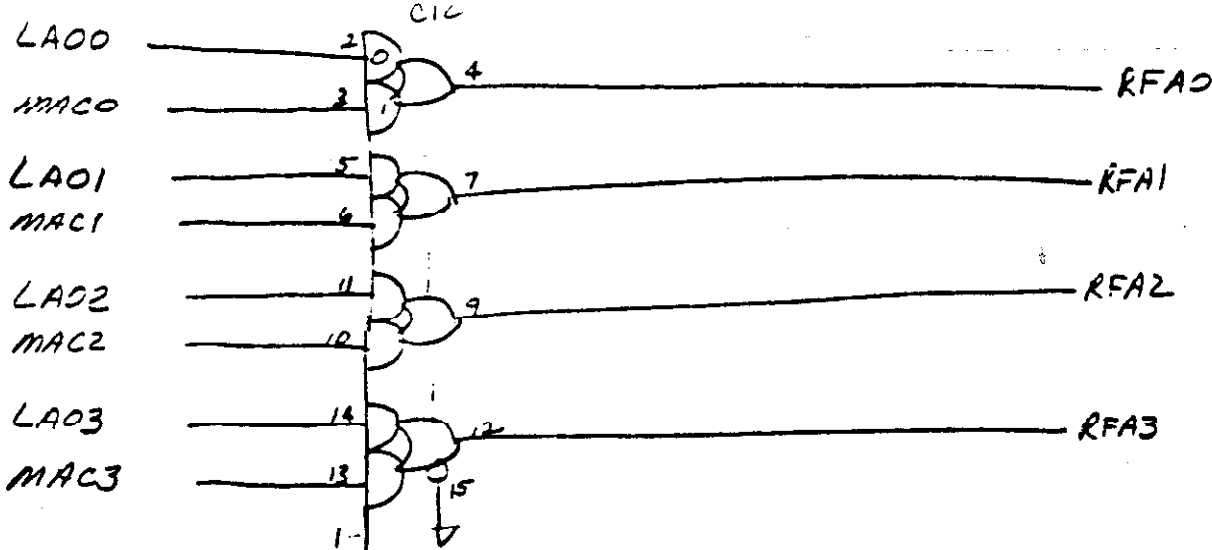


MAC4

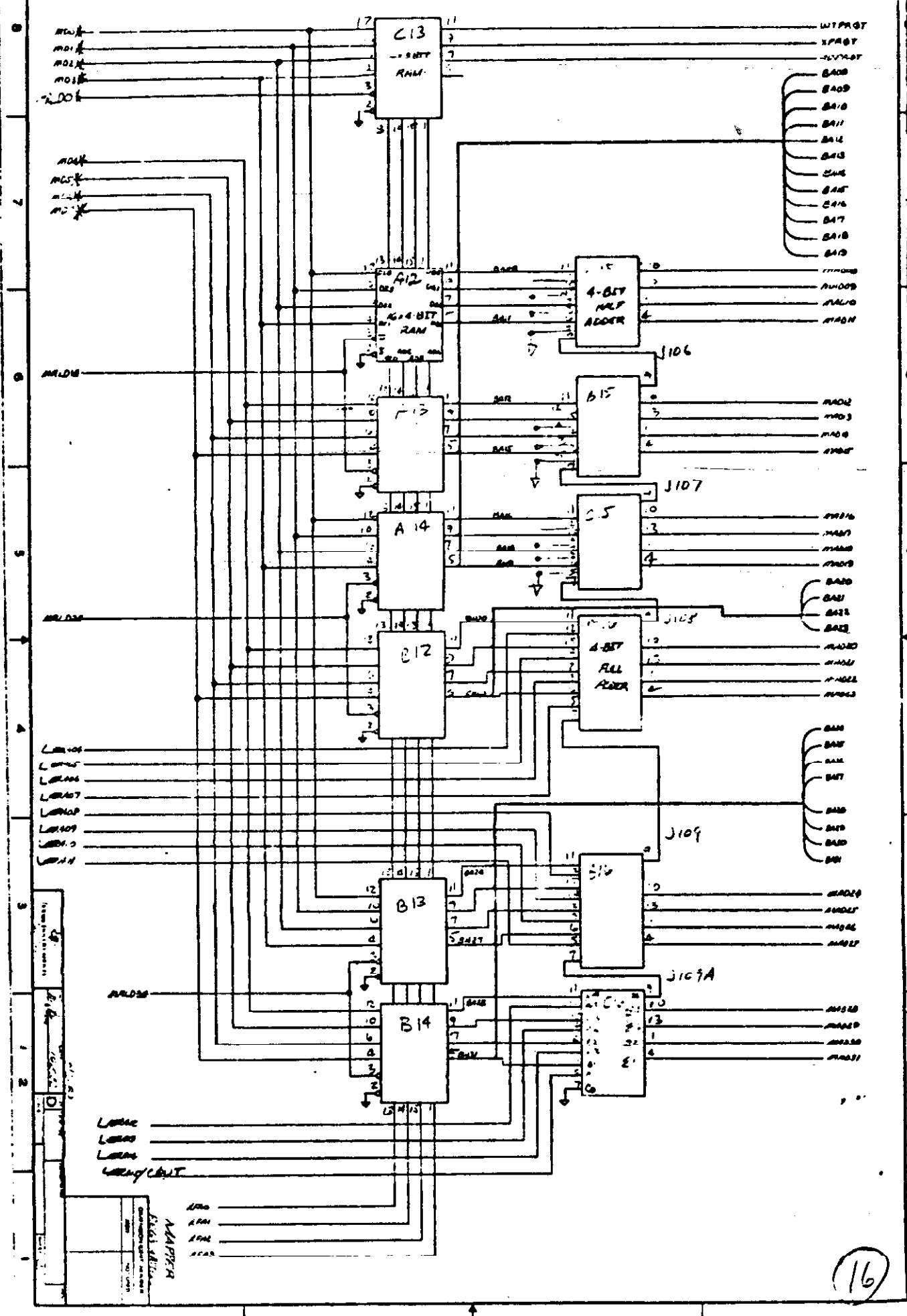
DMAC state Counter, Memory Load Store

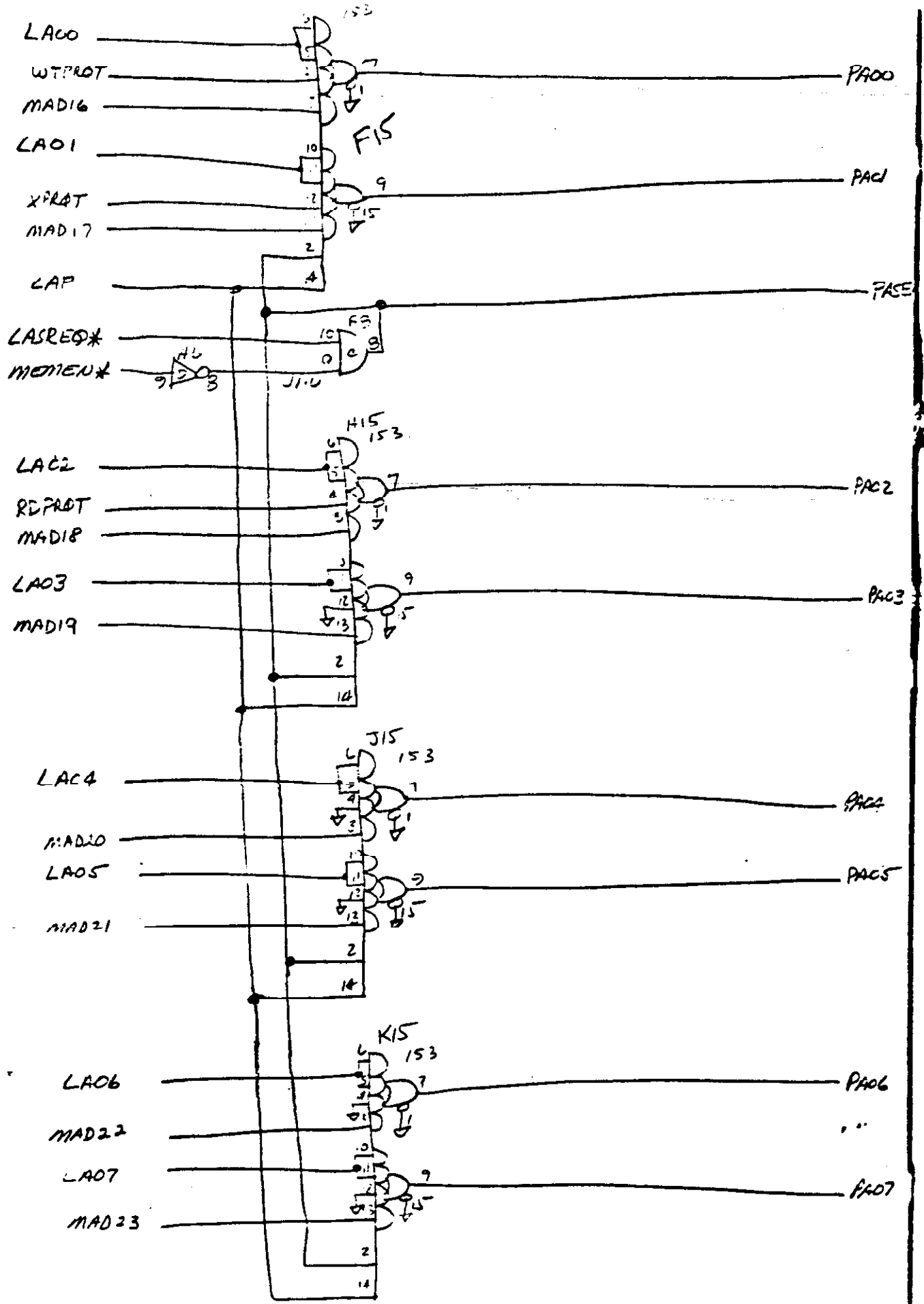


M. Appel



Mapper

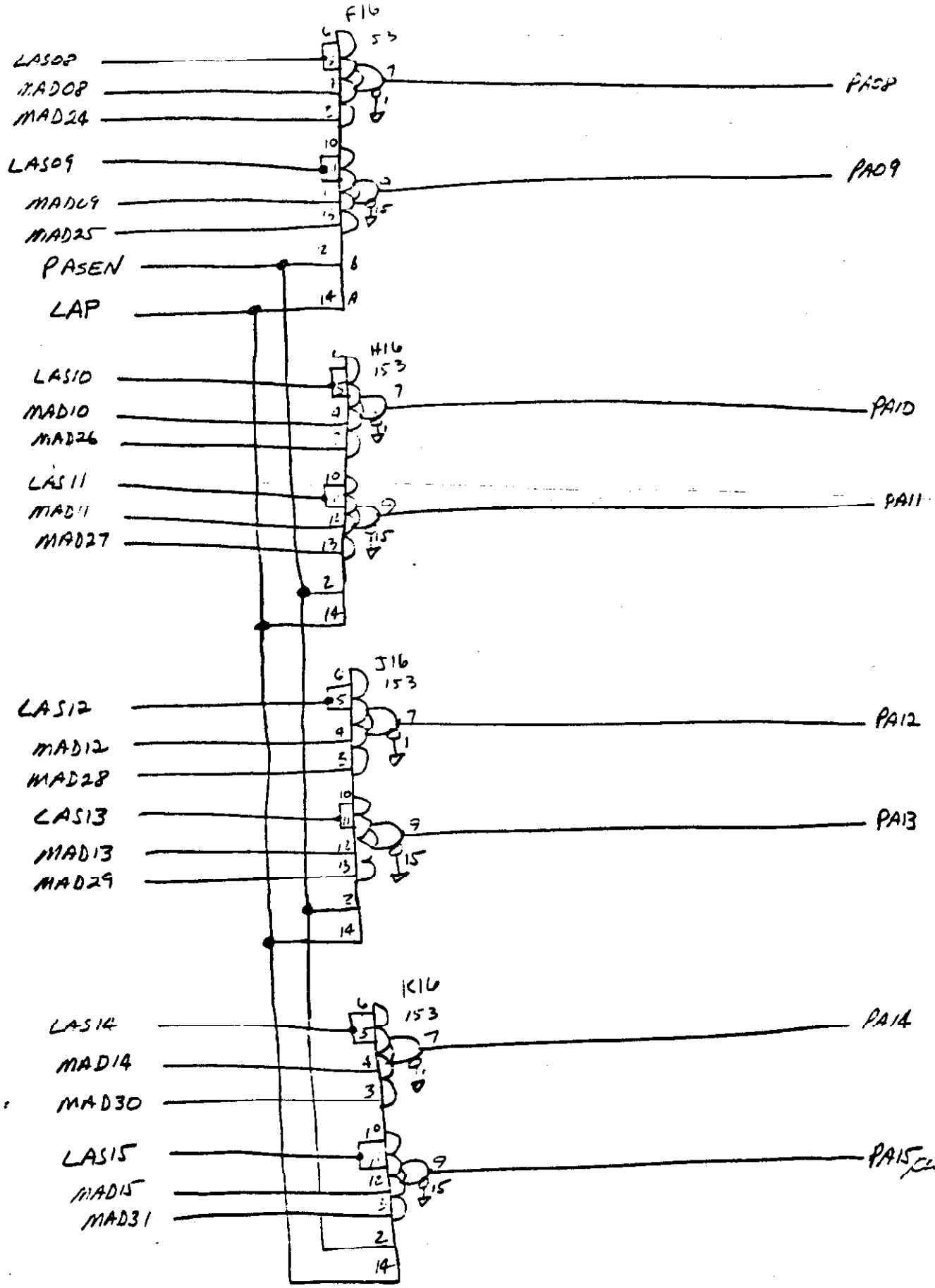




WIPPER

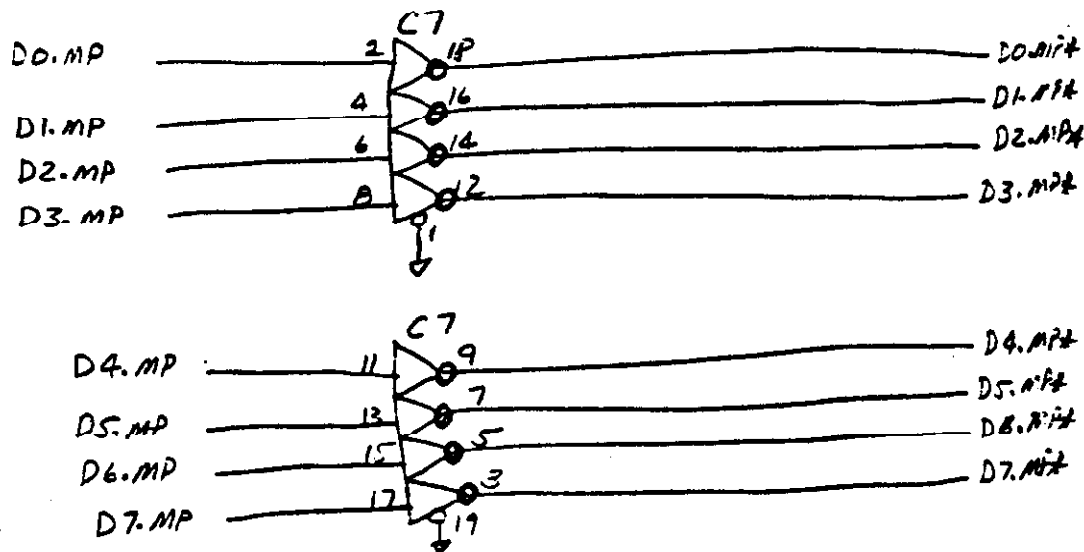
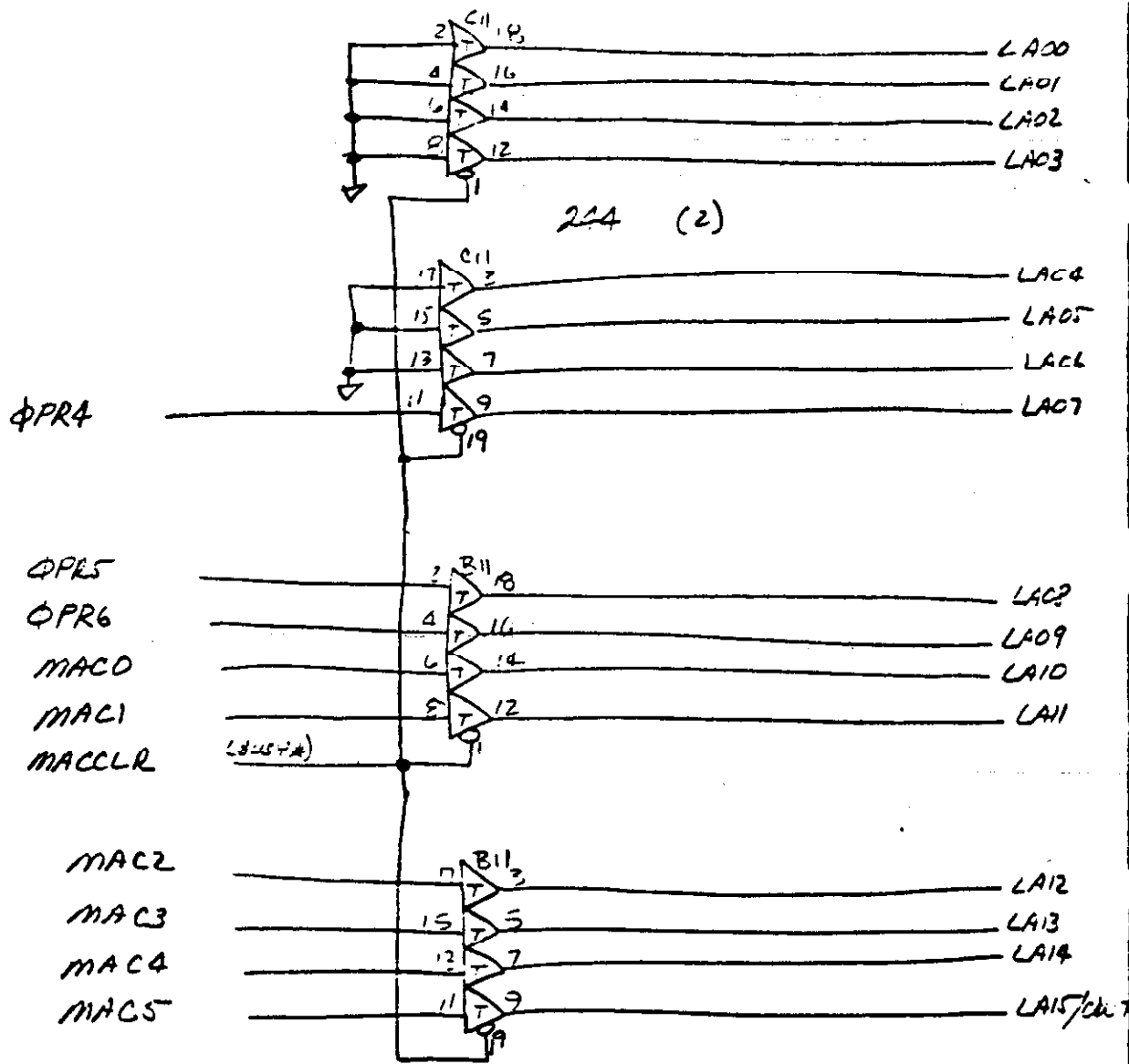
LAS/PAS MUX MSBY

(17)



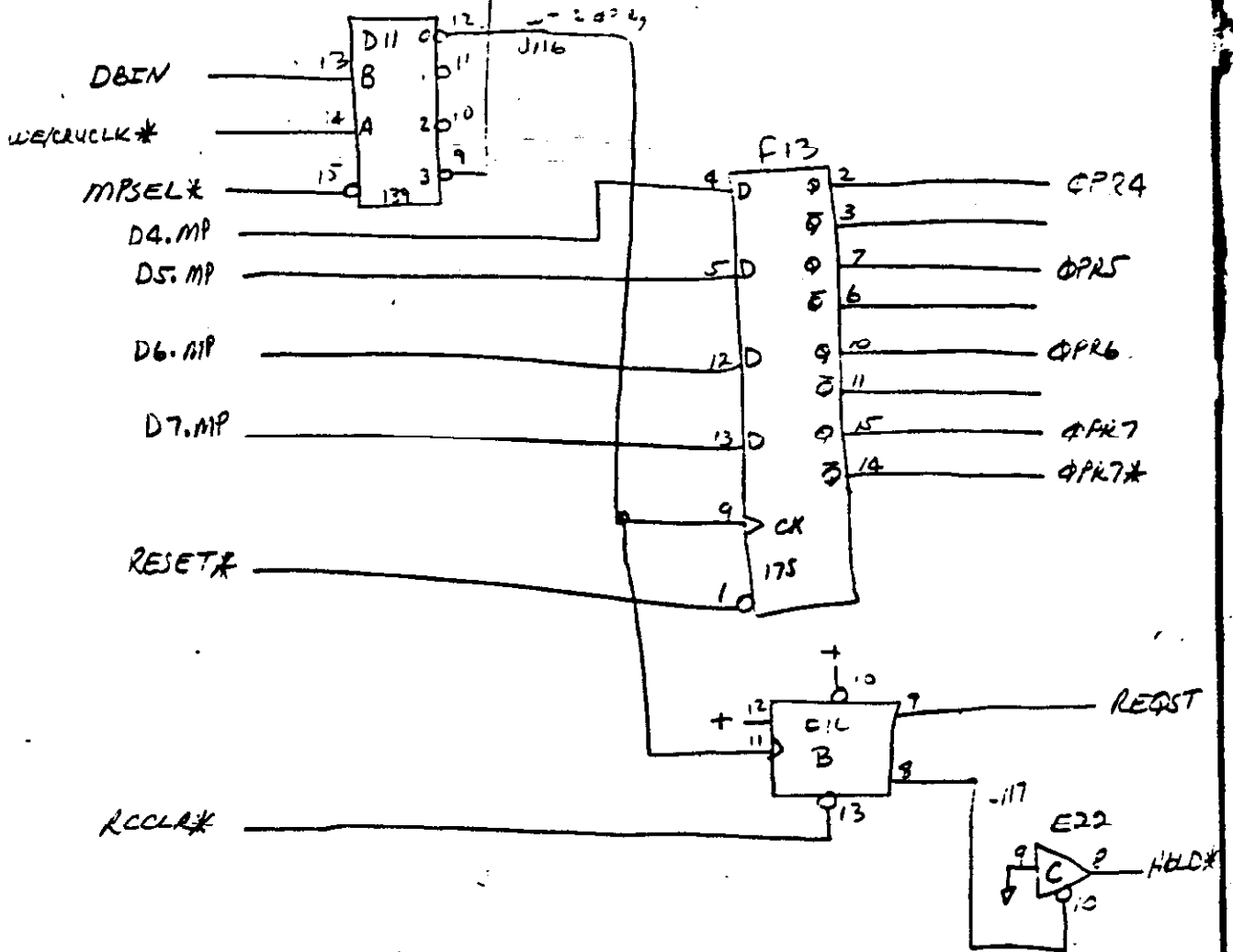
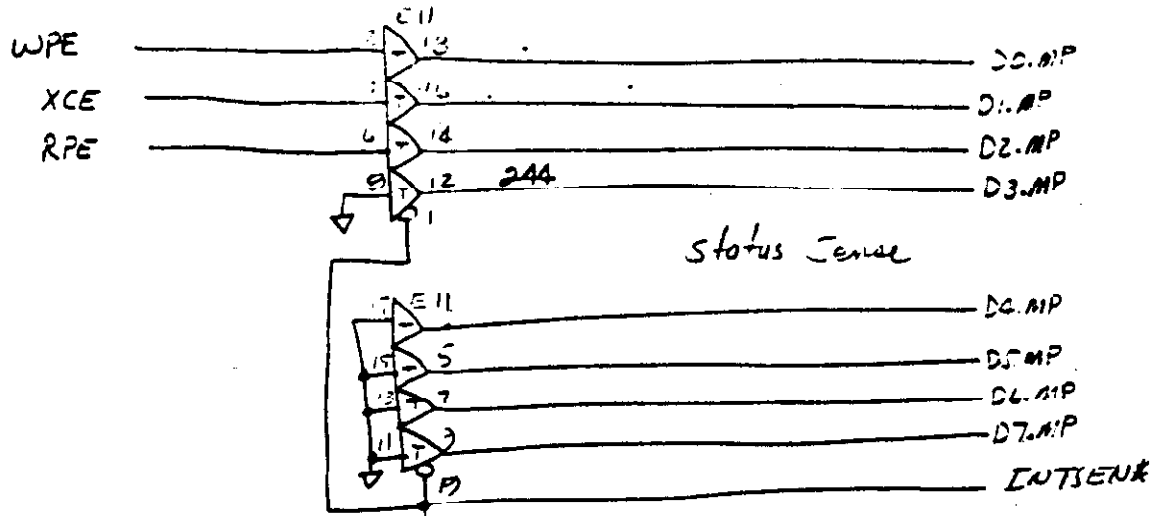
WIPPER

LAS/PAS MUX LSB4



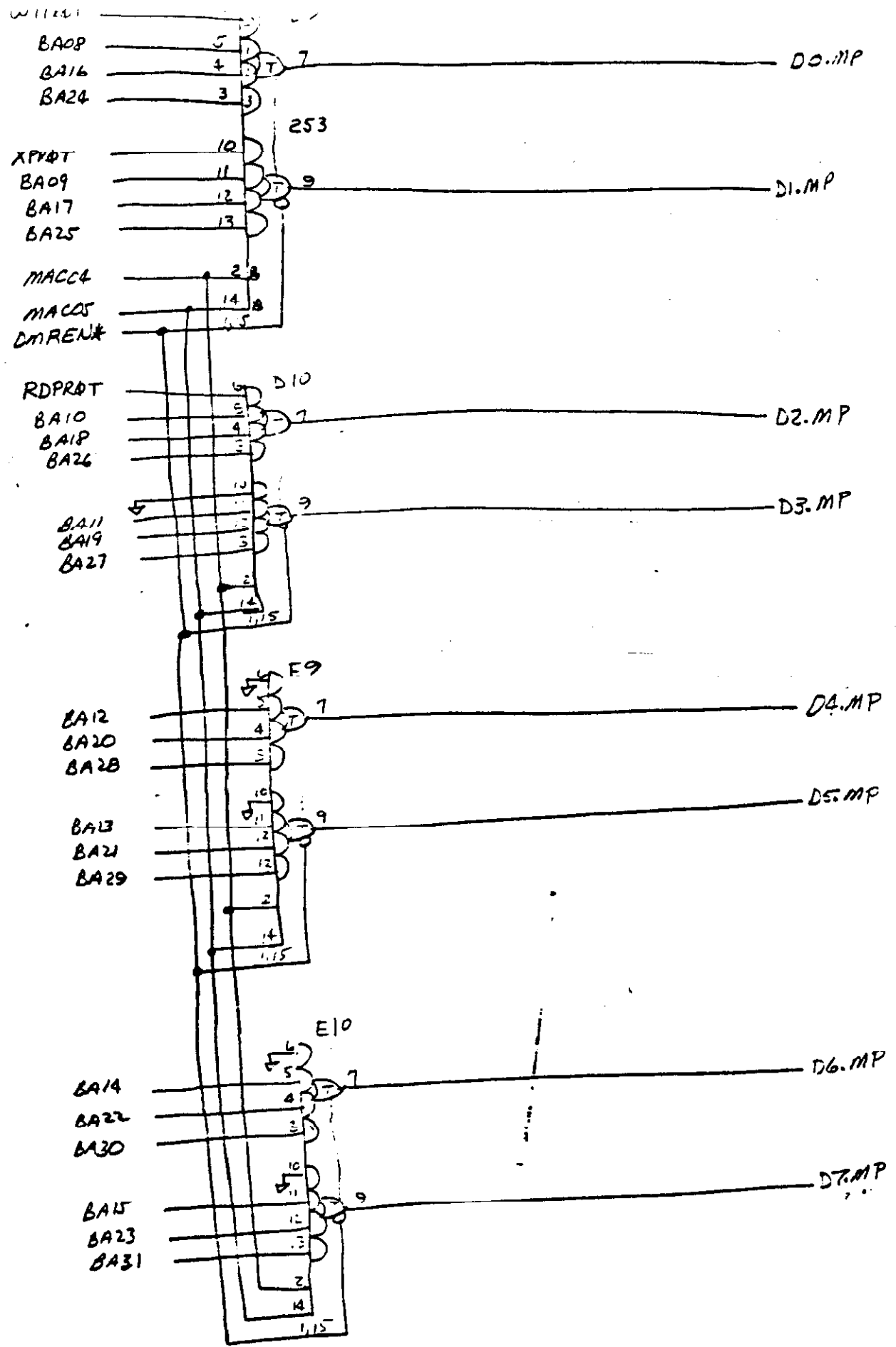
MAPPER

DMA Address Drivers



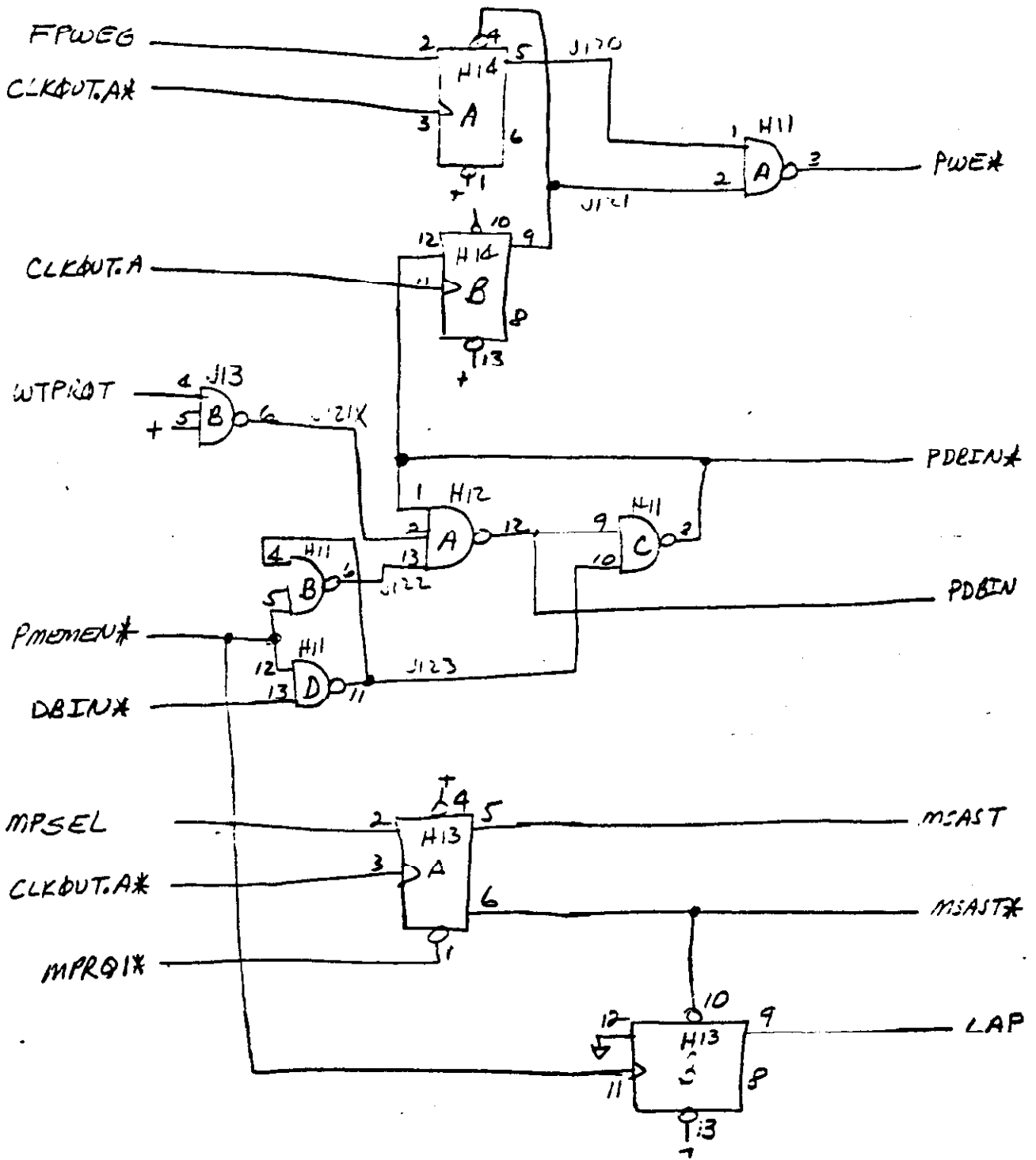
iii

Status Sense, OP R7



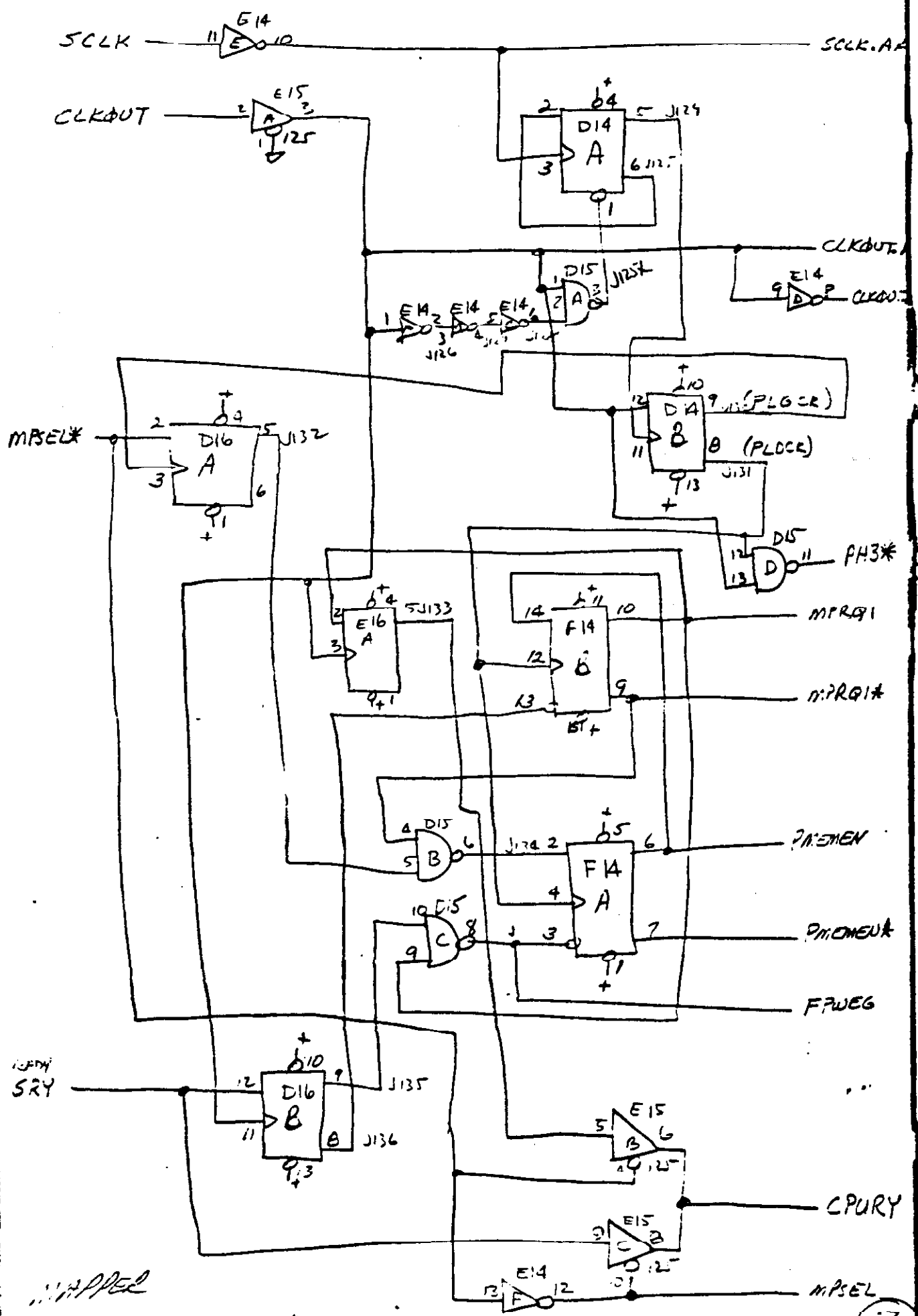
W. L. L. P. E. R.

DMA READ MUX



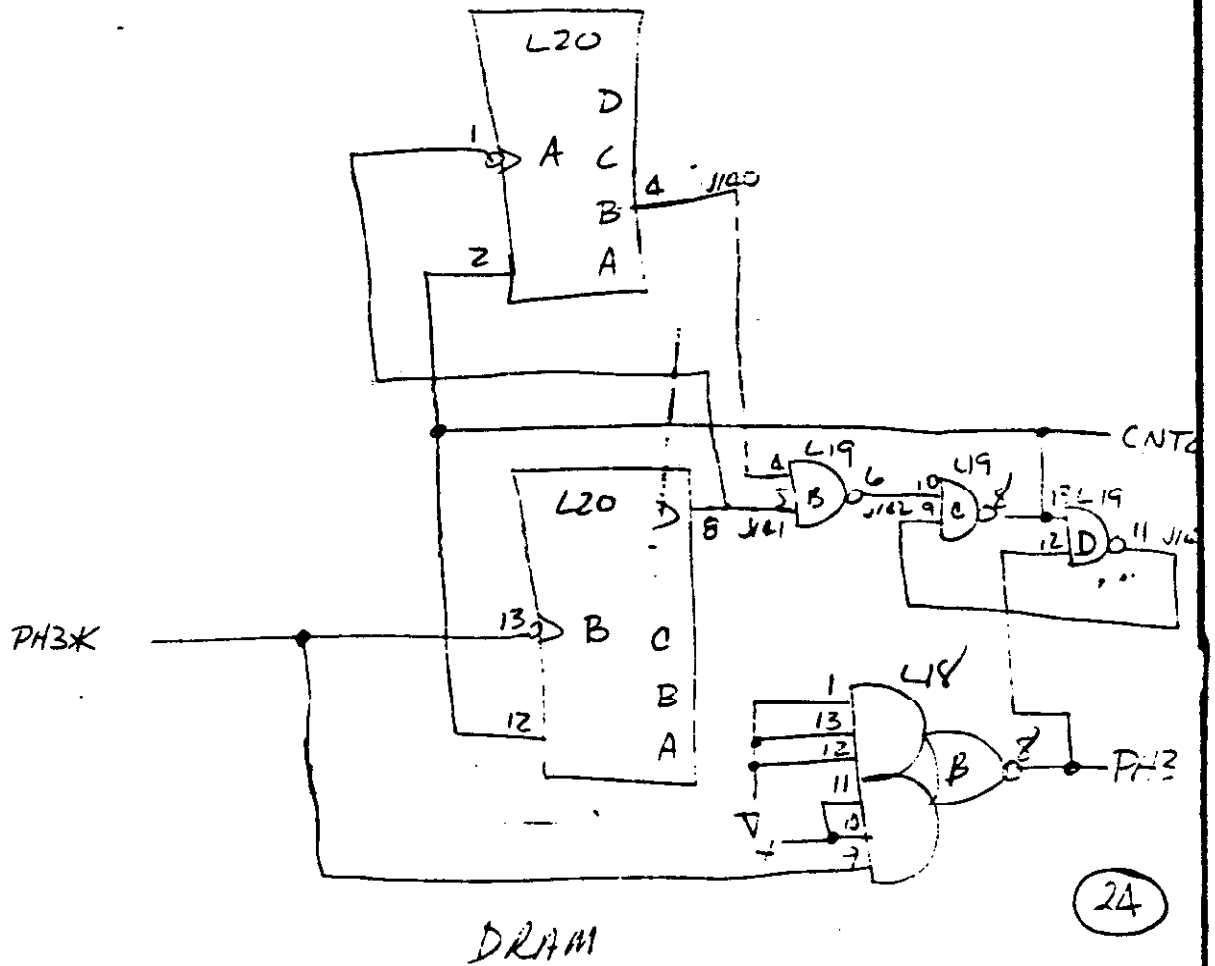
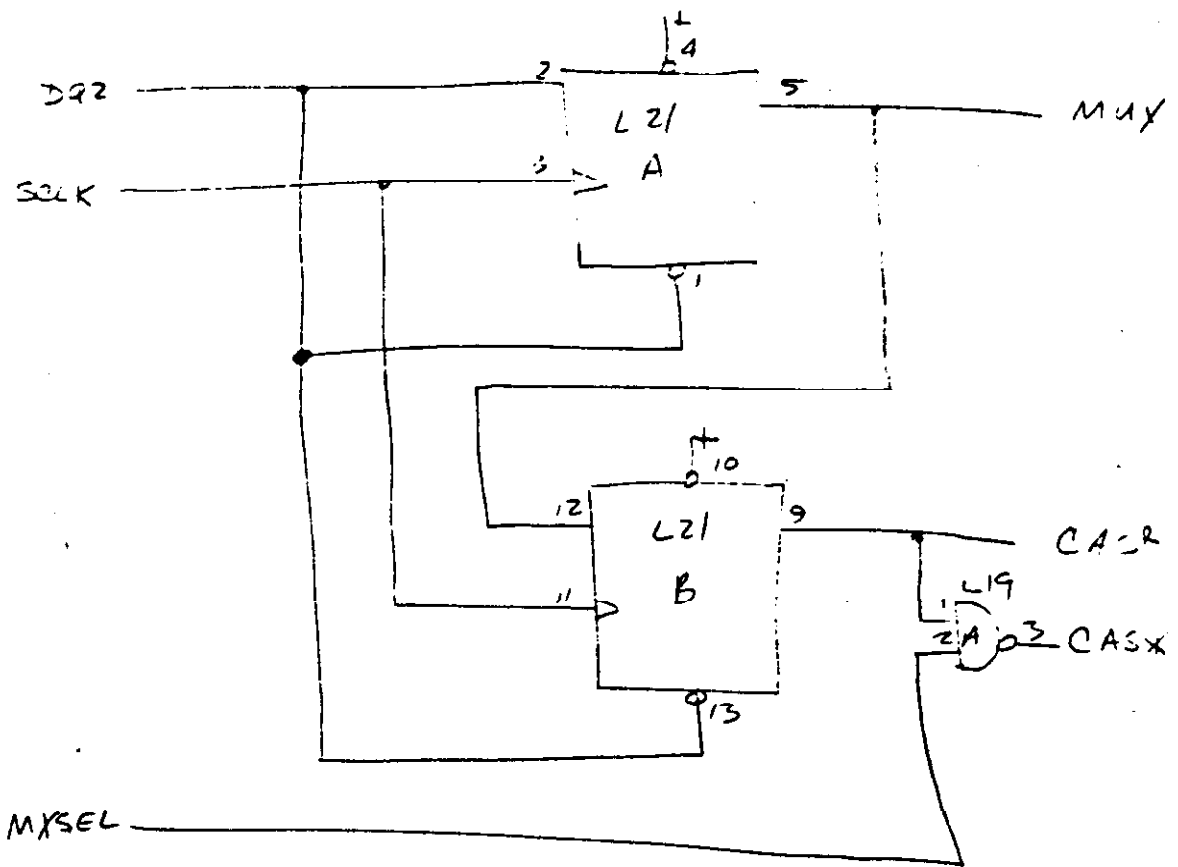
Ulfjose

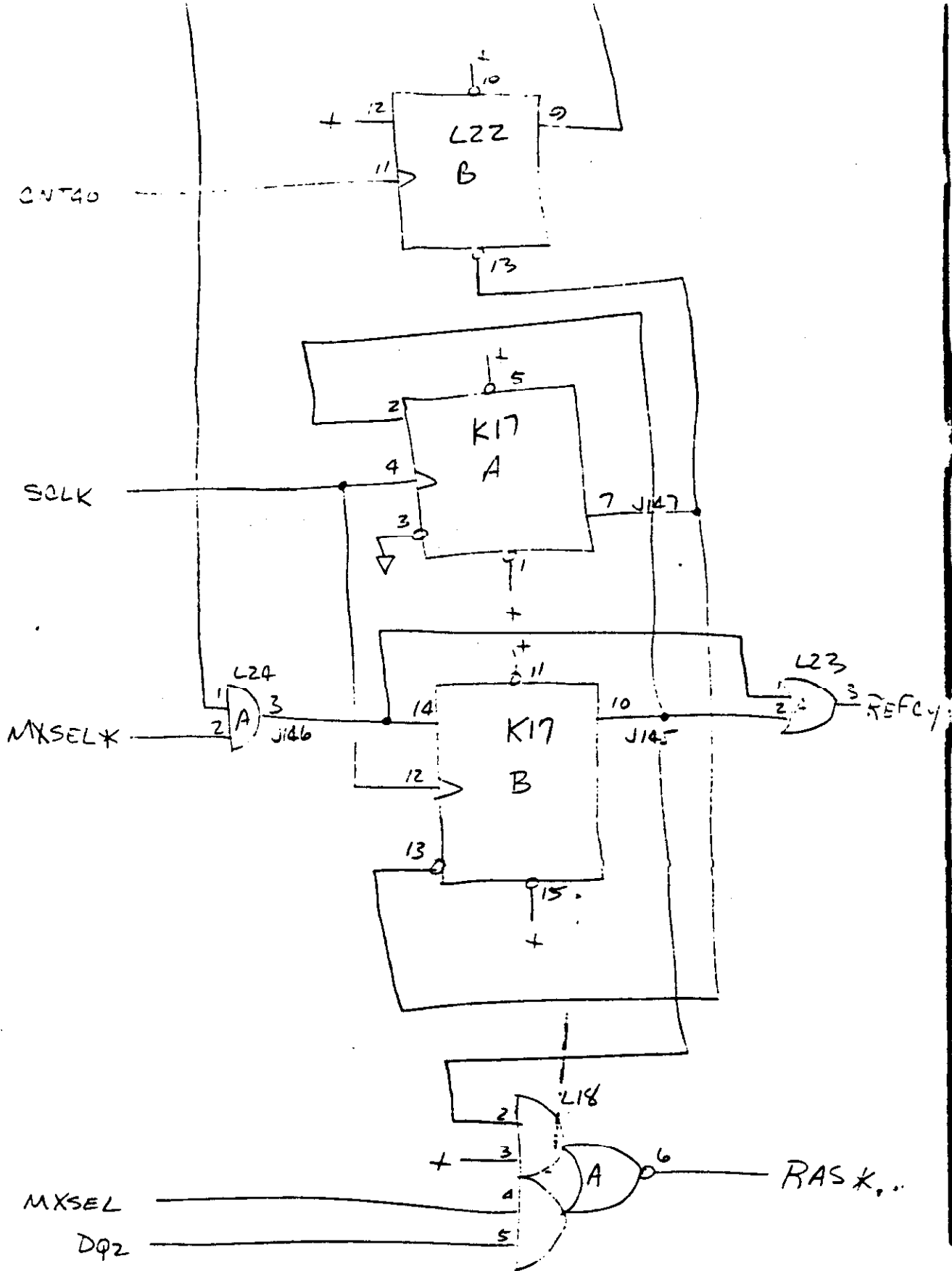
"P" Signal Gen #2



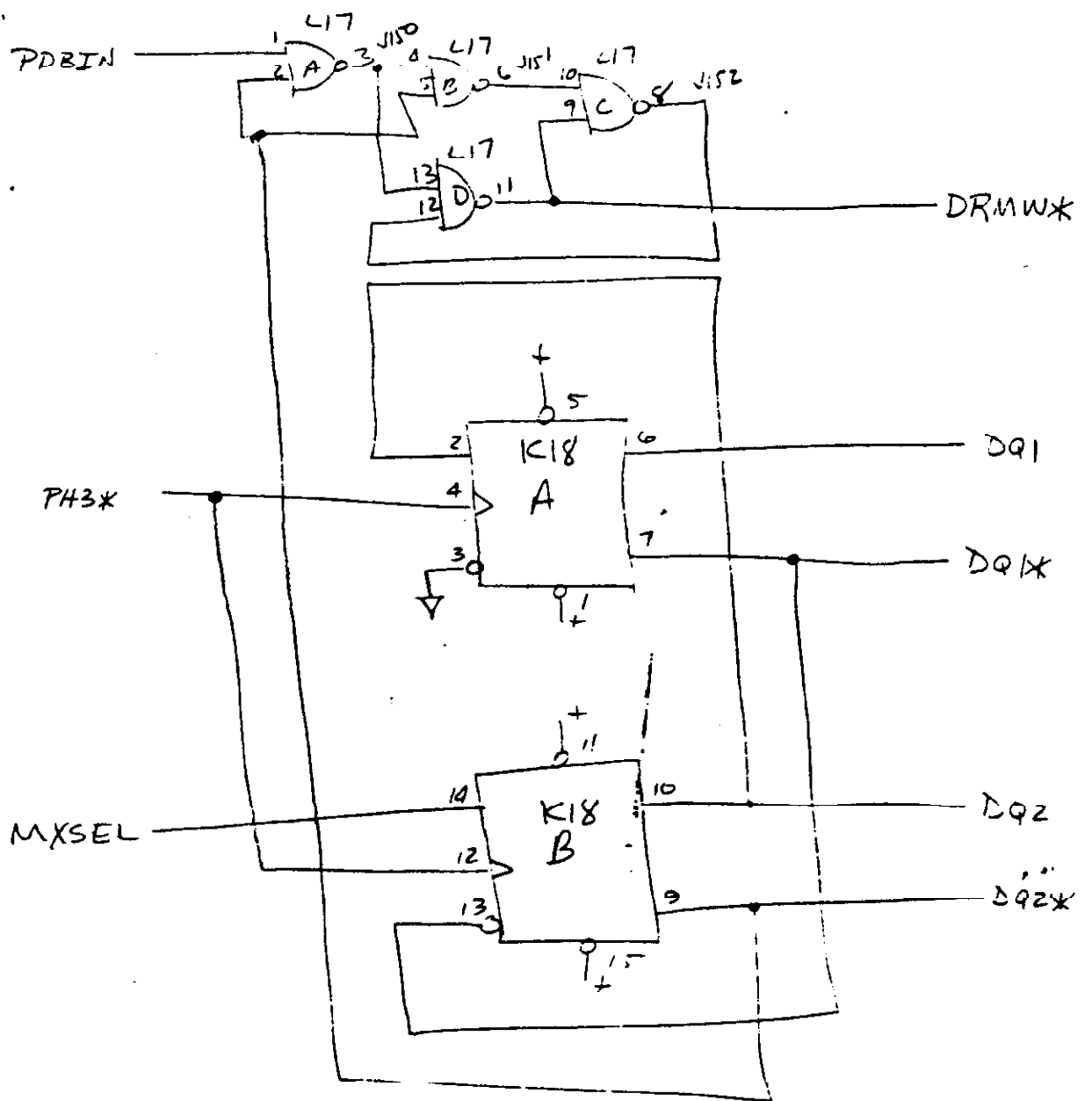
MAPPER

TTC "P" Signals



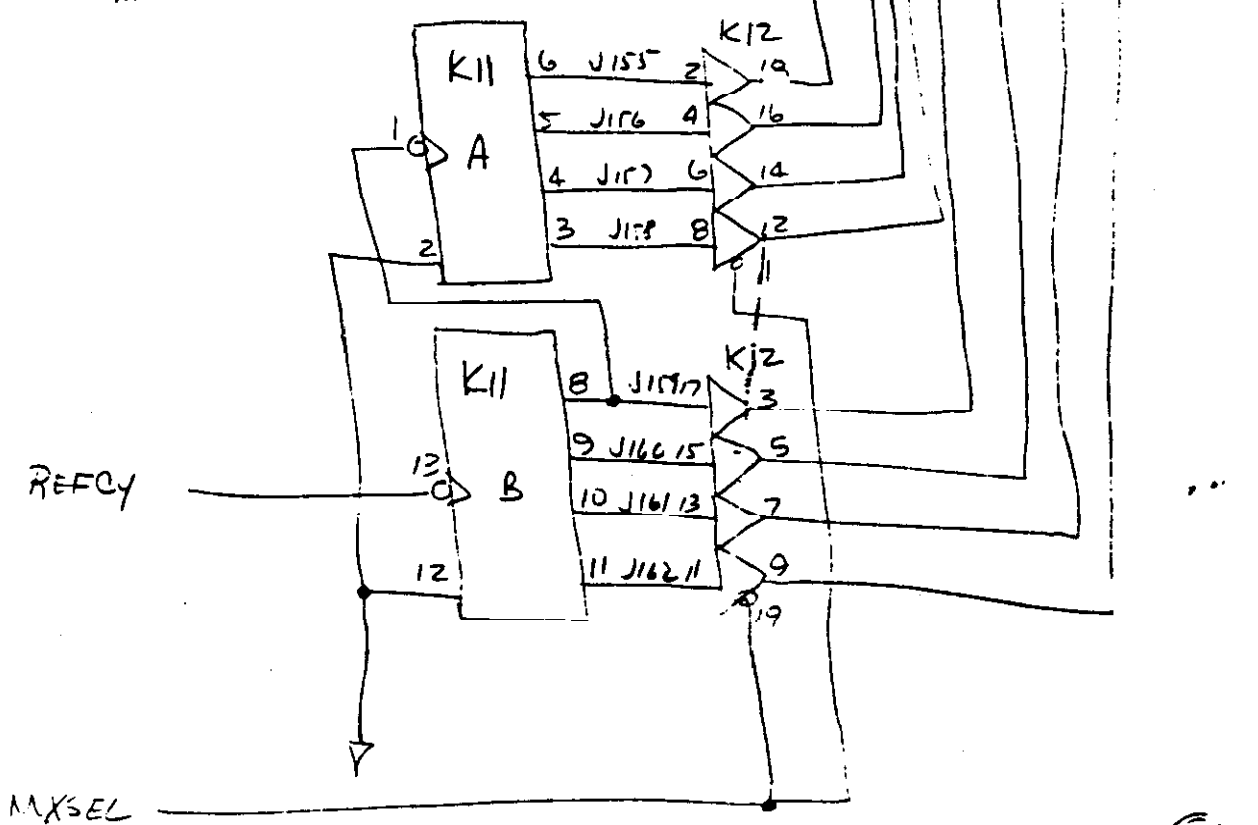
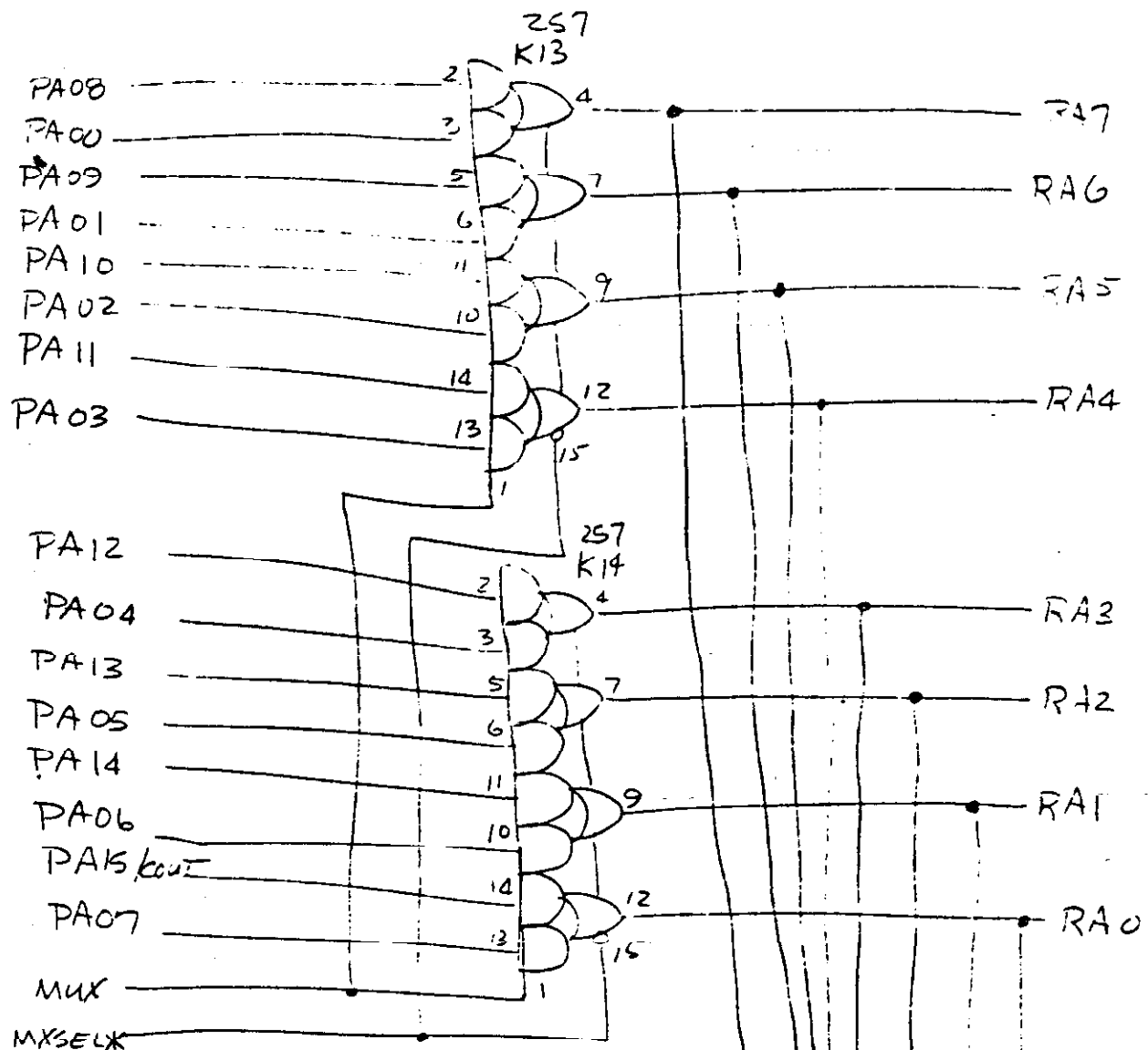


DRAWN

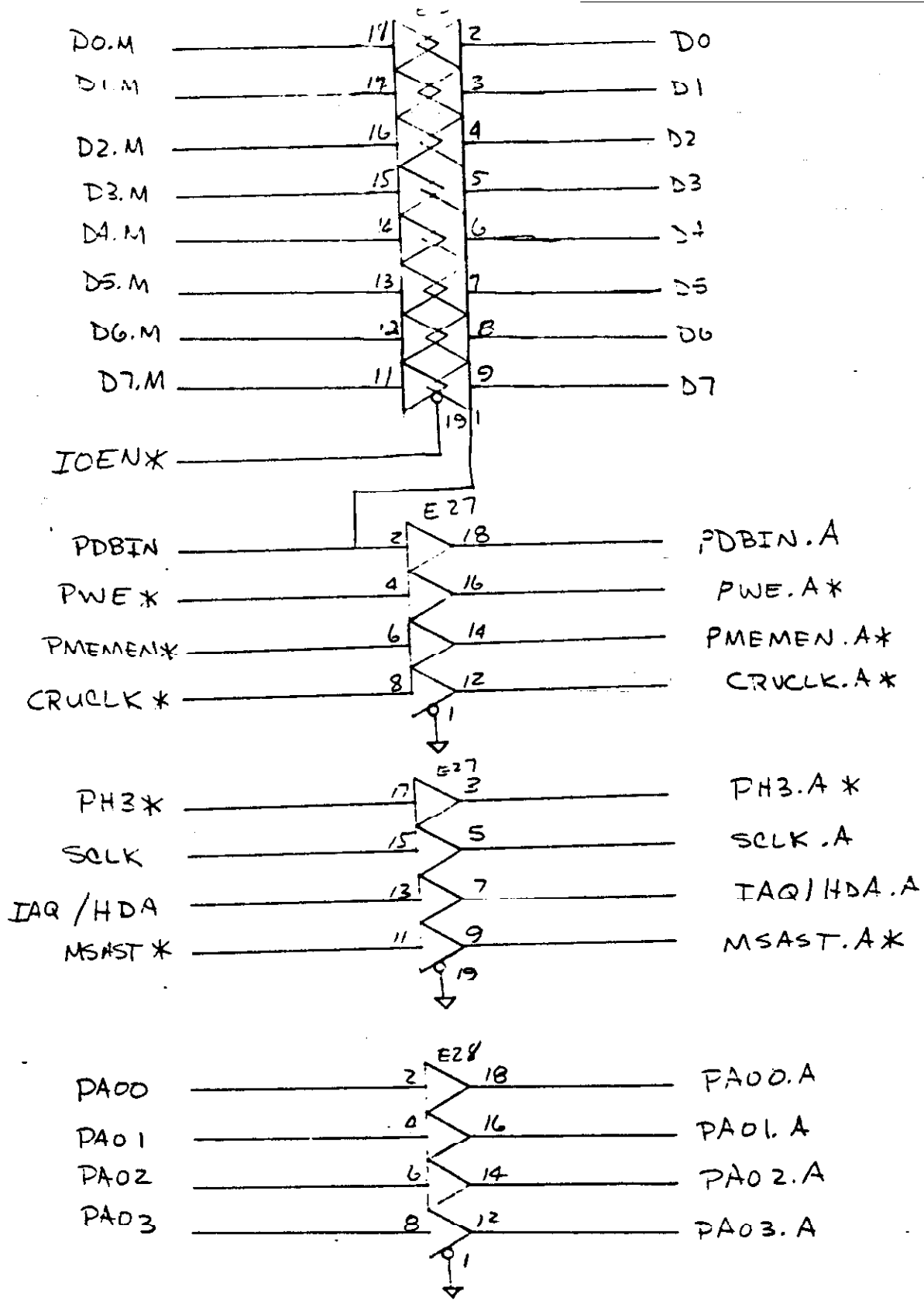


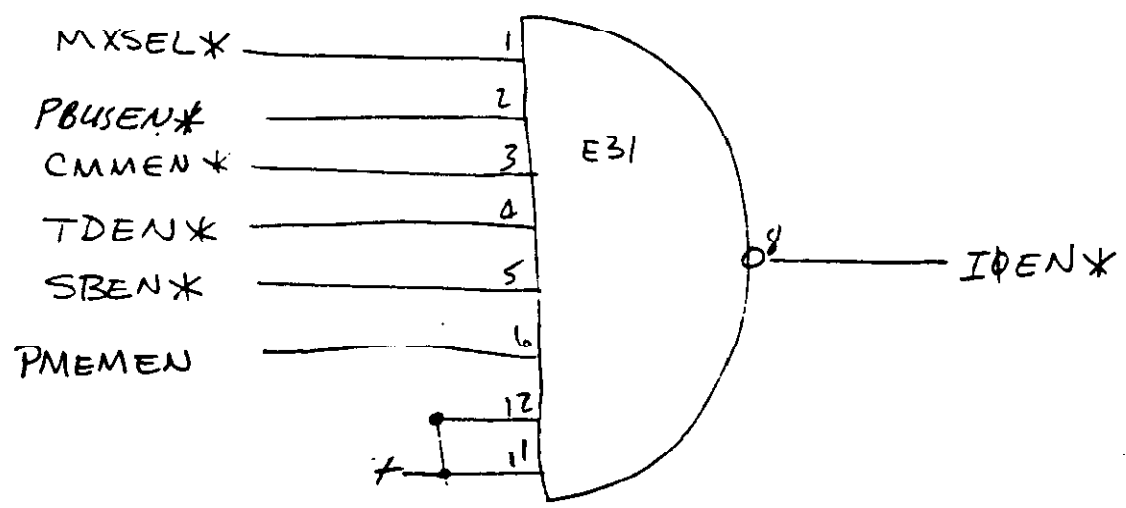
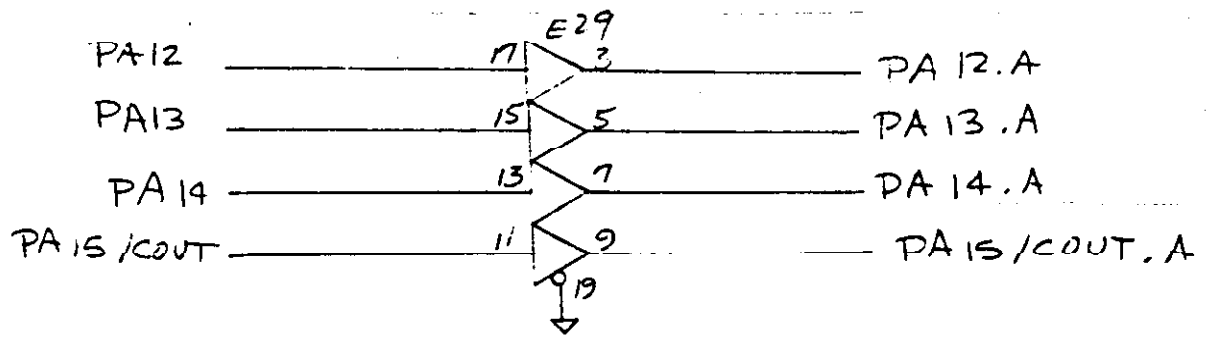
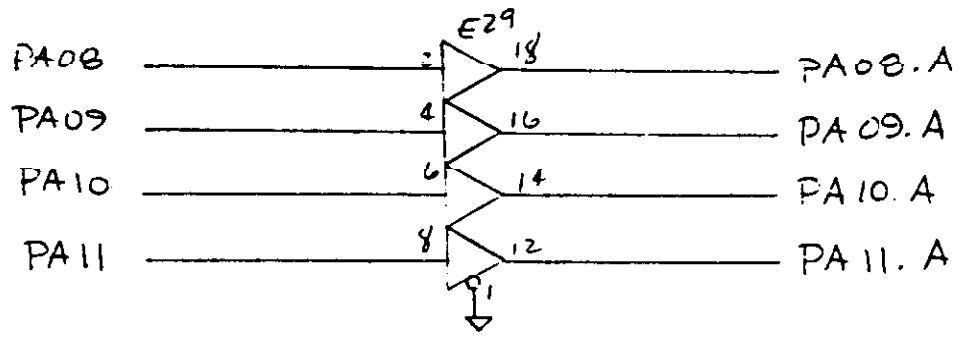
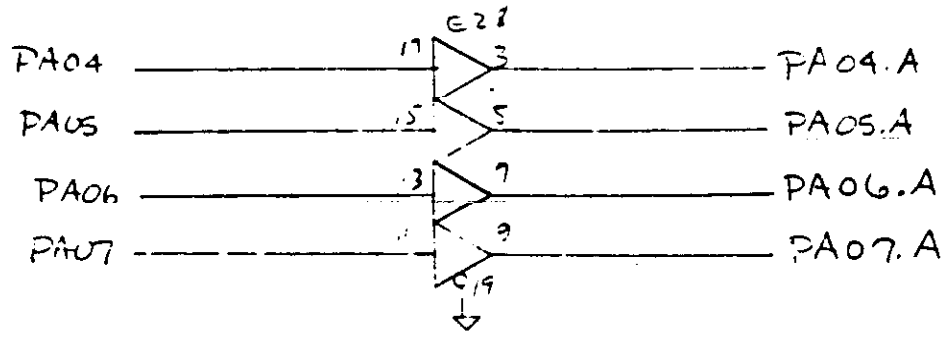
DRAWN

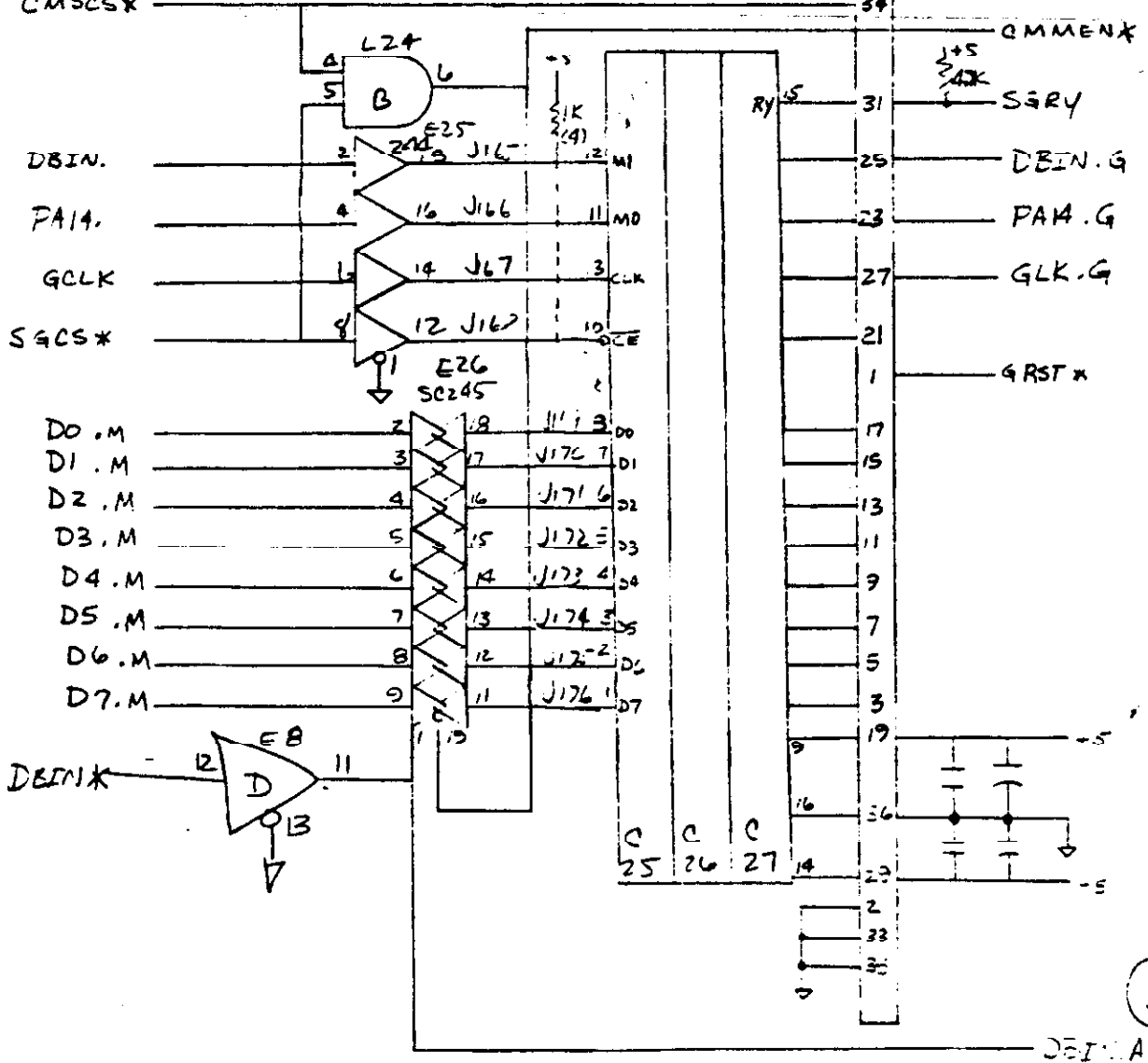
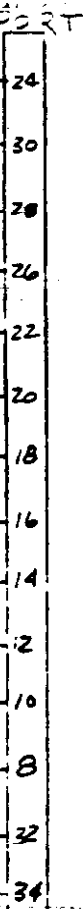
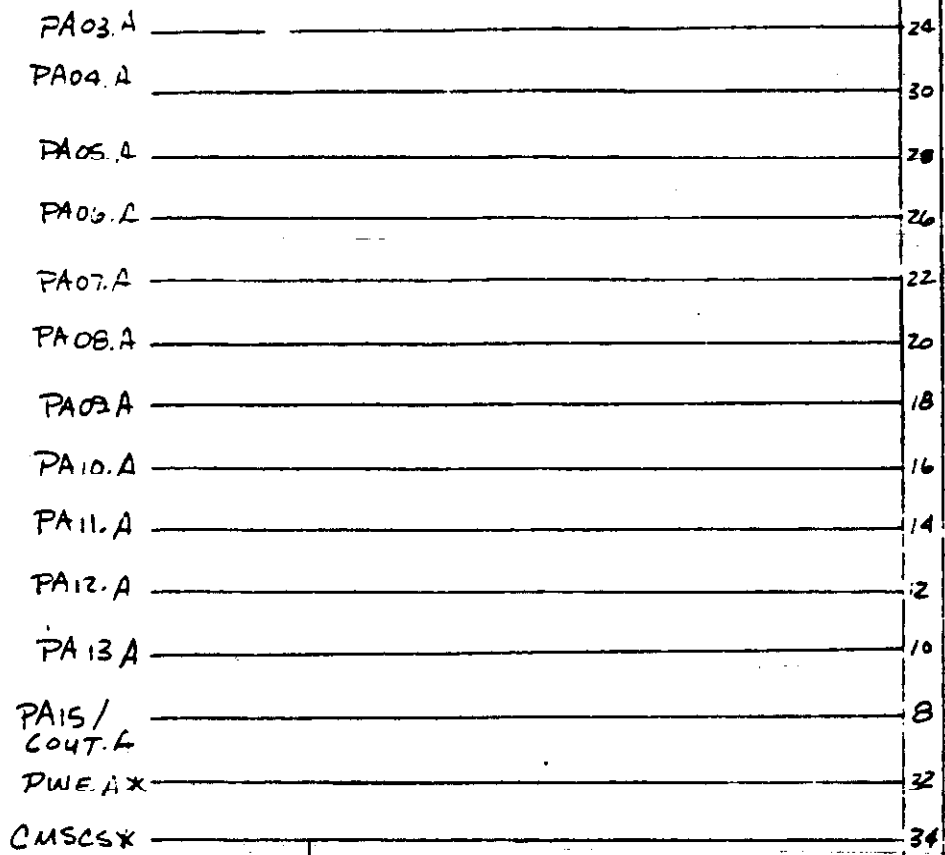
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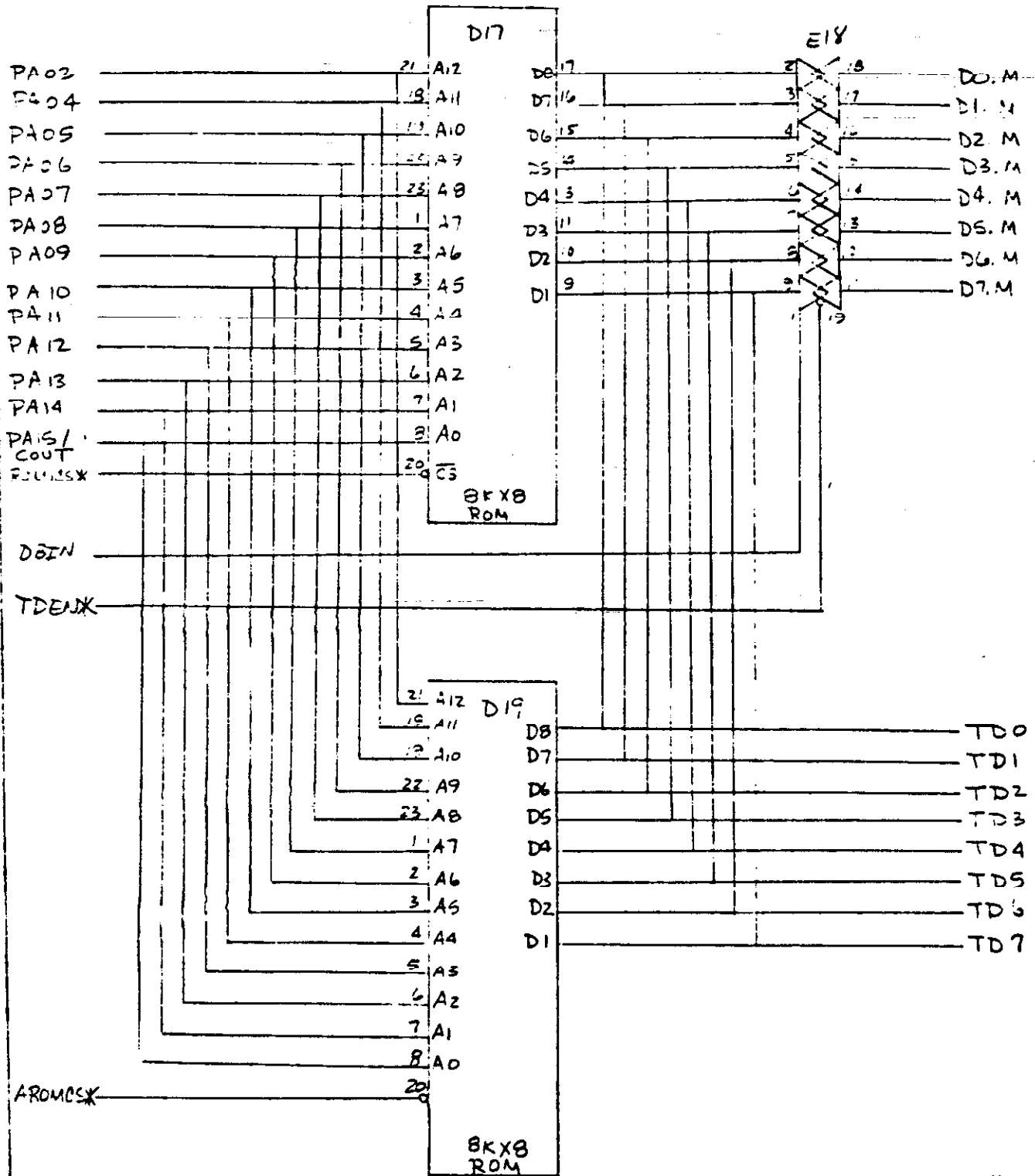


DRAM



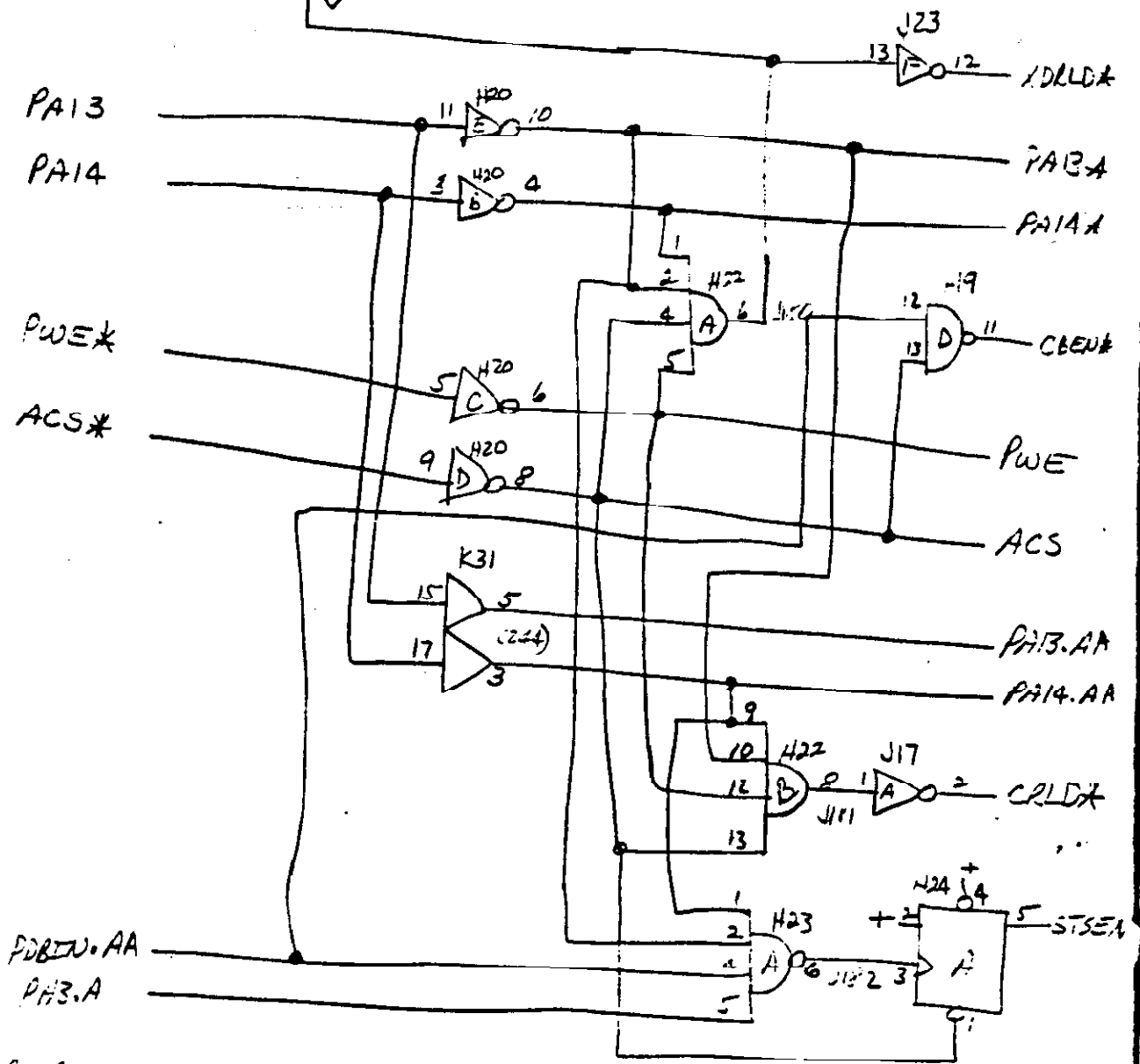
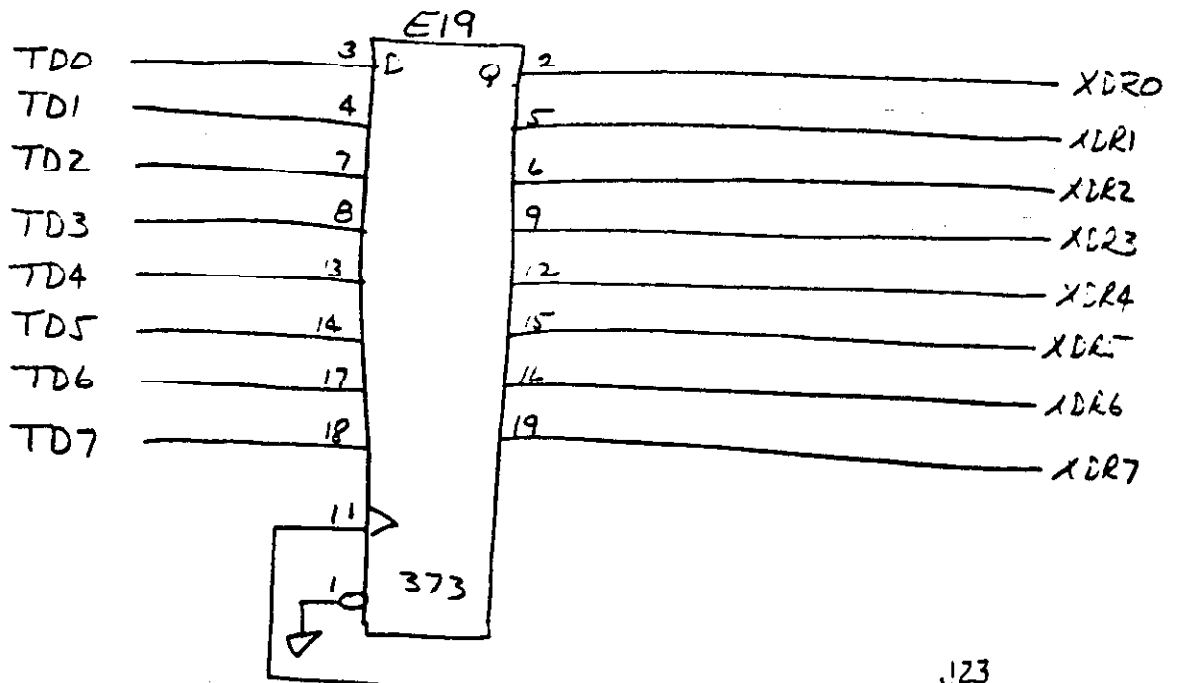






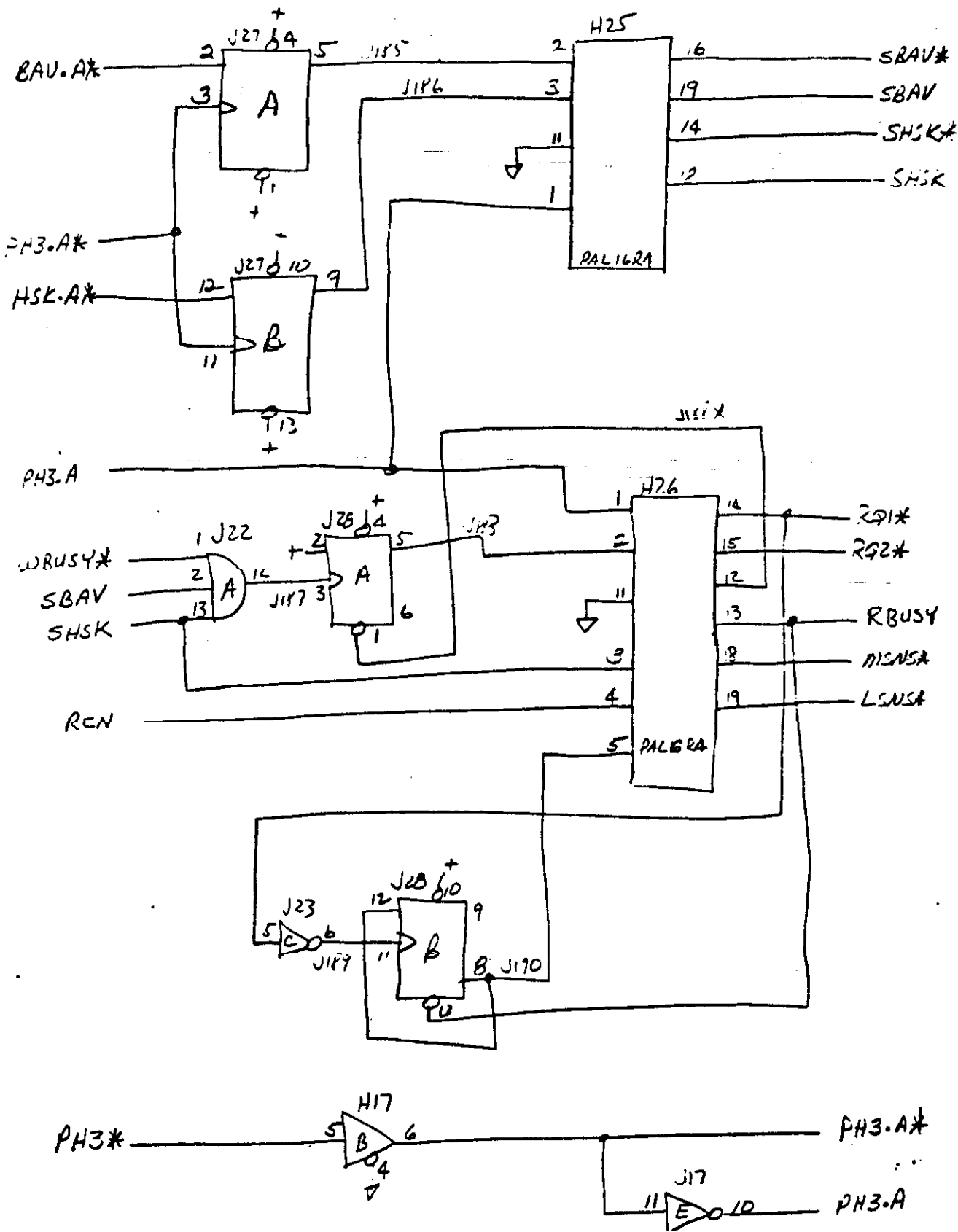
PAS ROM

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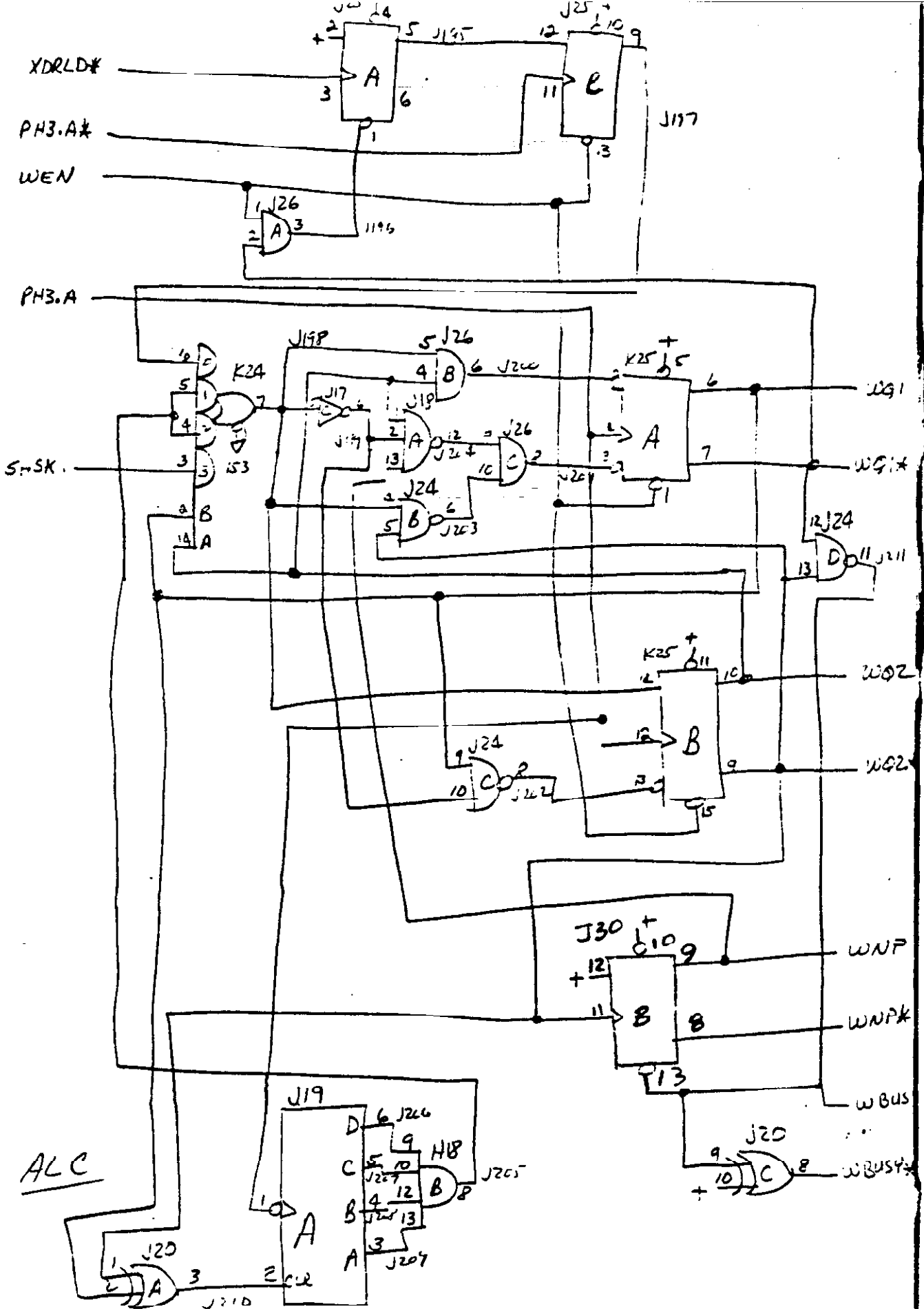
ALC

XMIT DR, Key Decodes

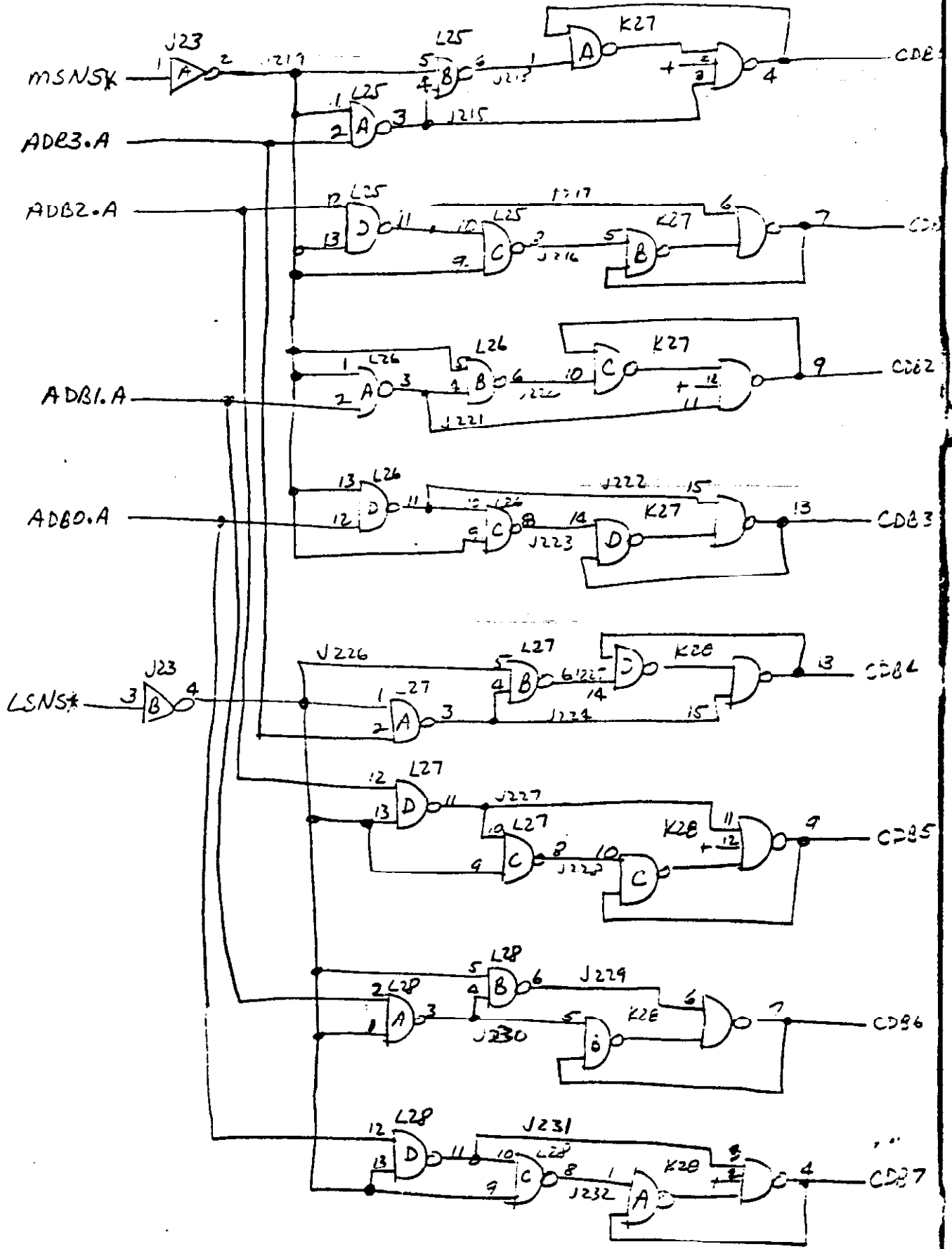


HLC

BAV, HSK Logic, READ state counter logic



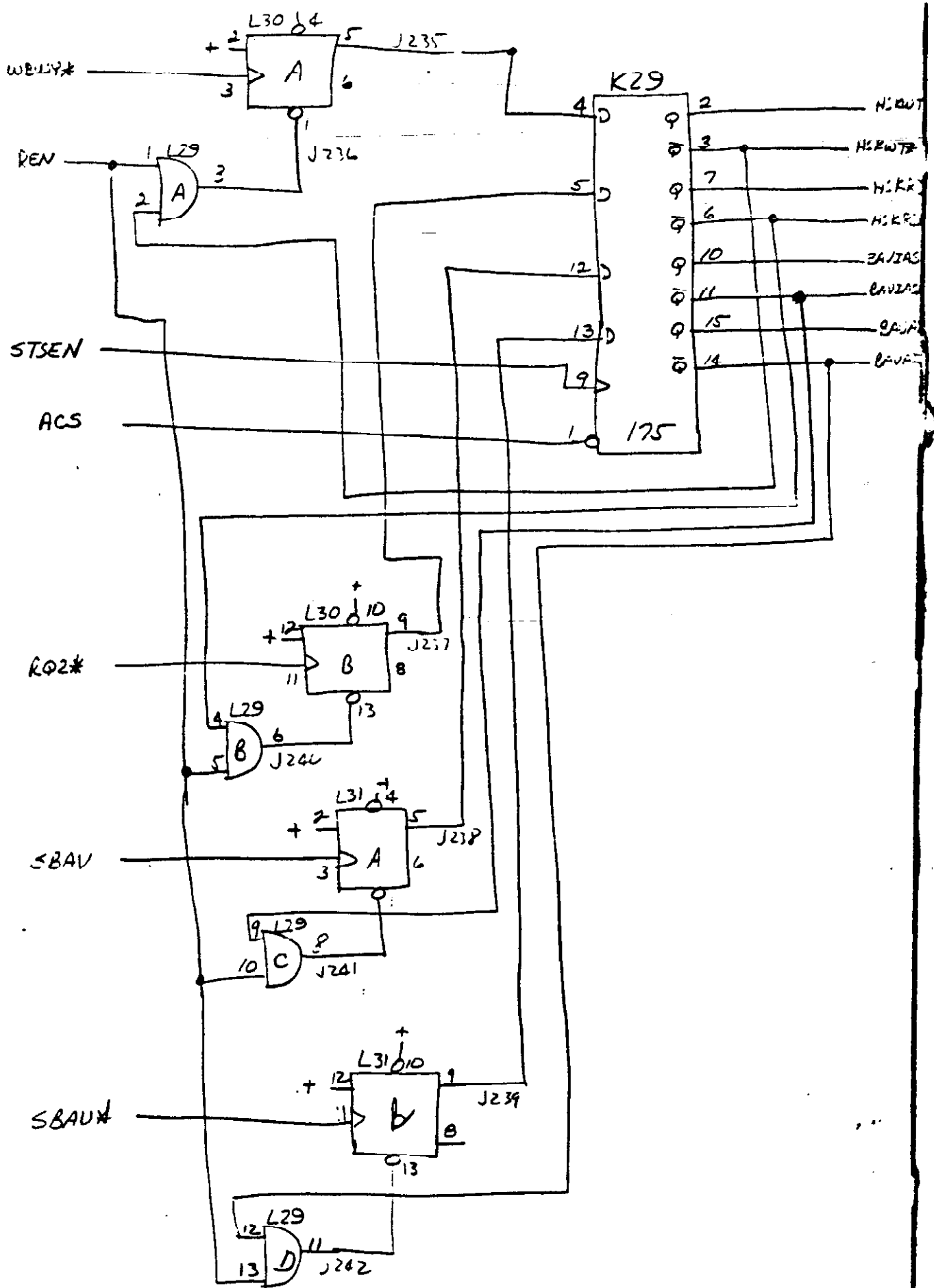
WRITE State Counter



ALC

ALC READ REG

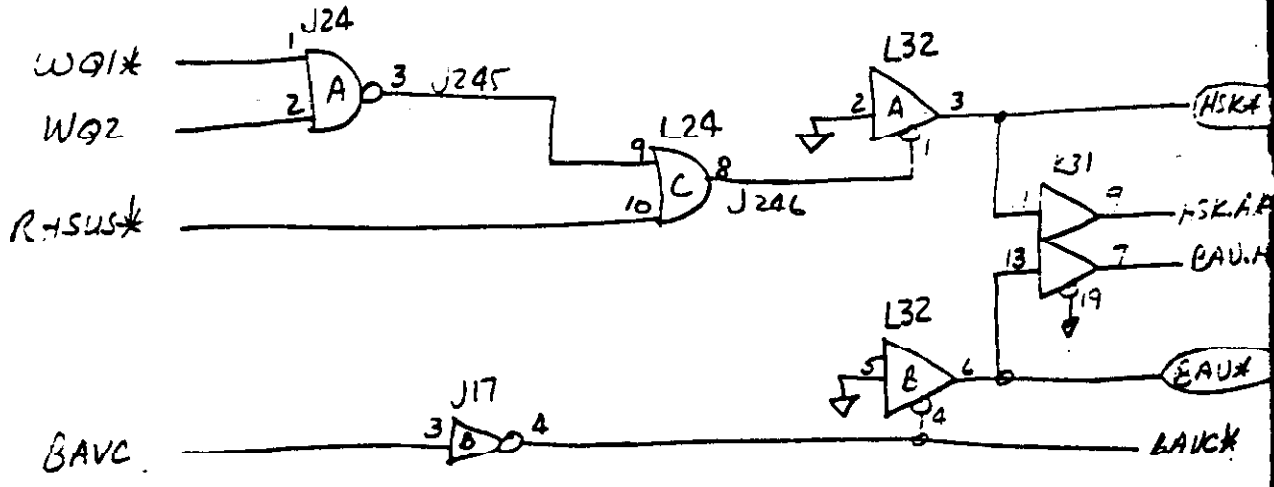
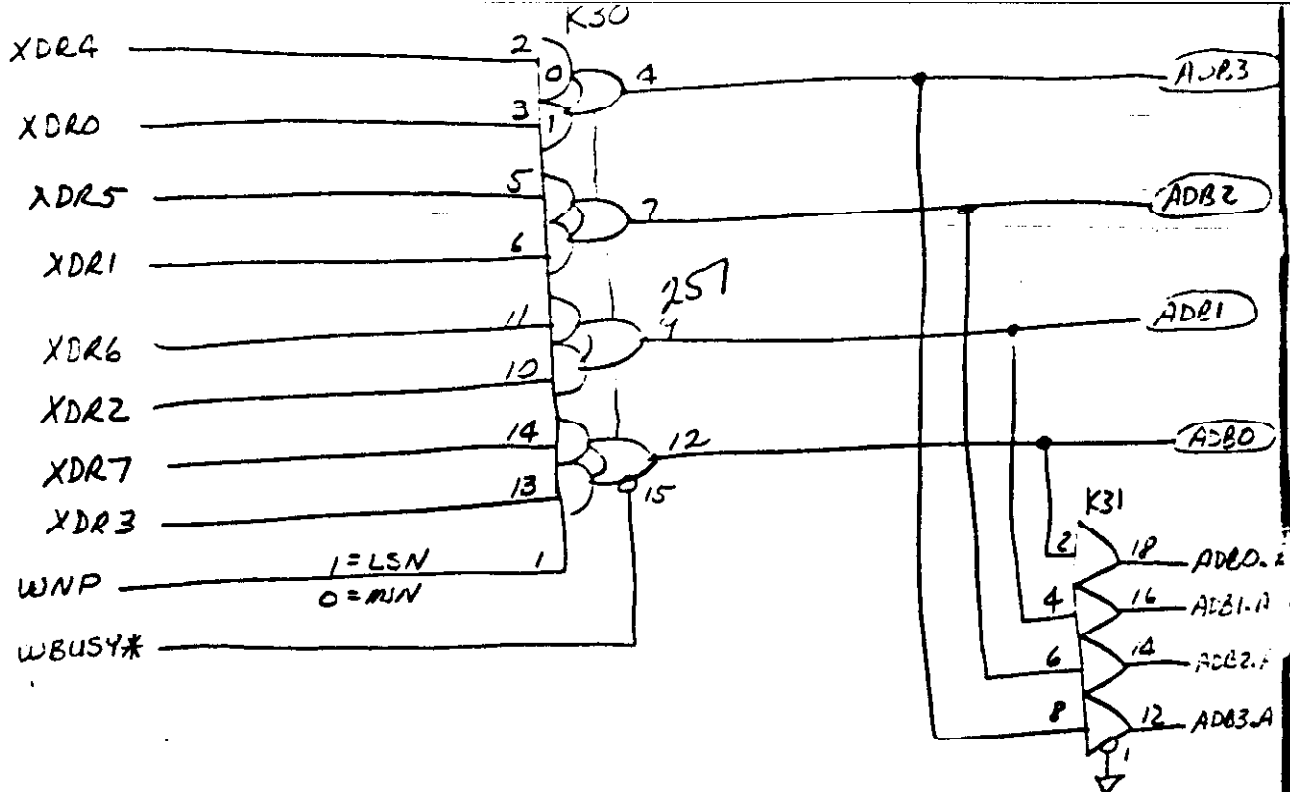




ALC

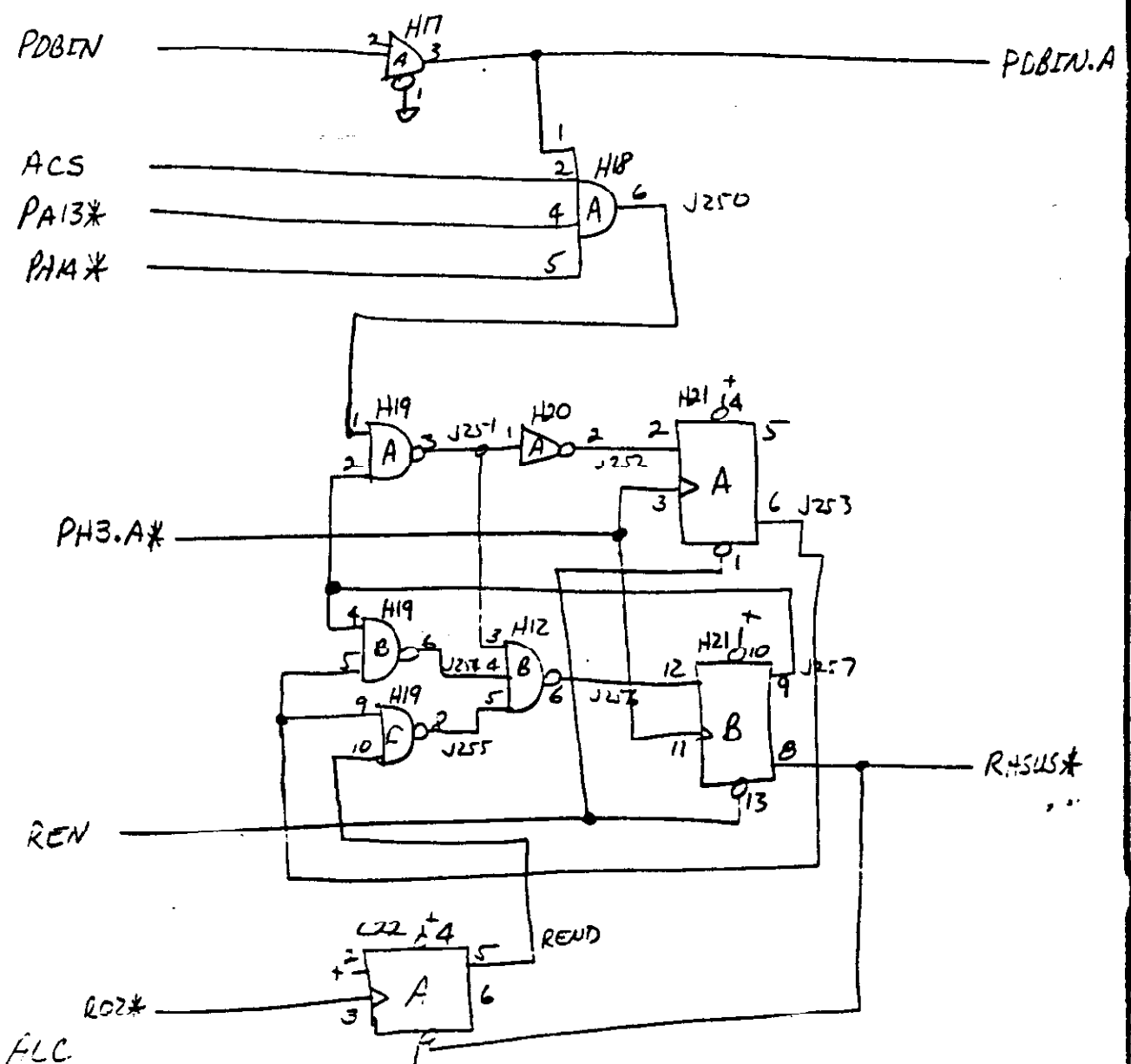
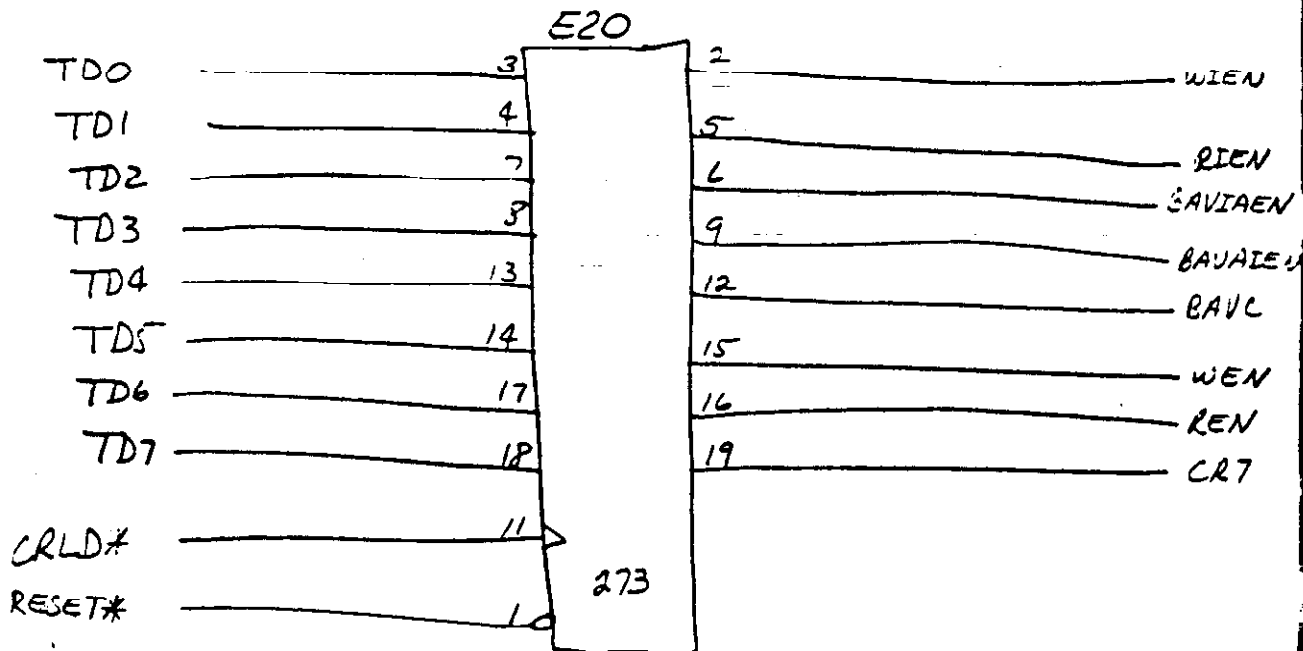
Status RQ2 Sense w/ RESET



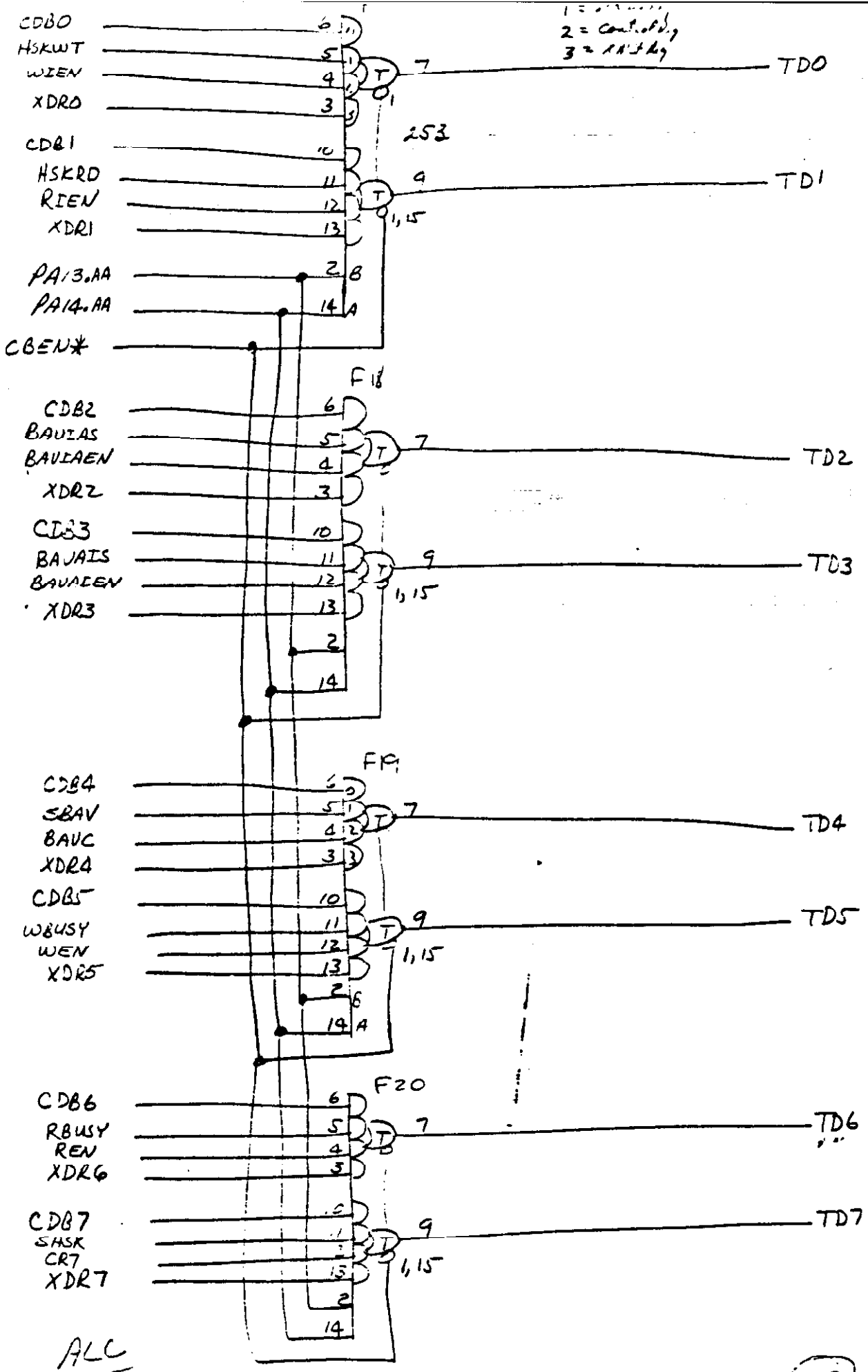


ALC

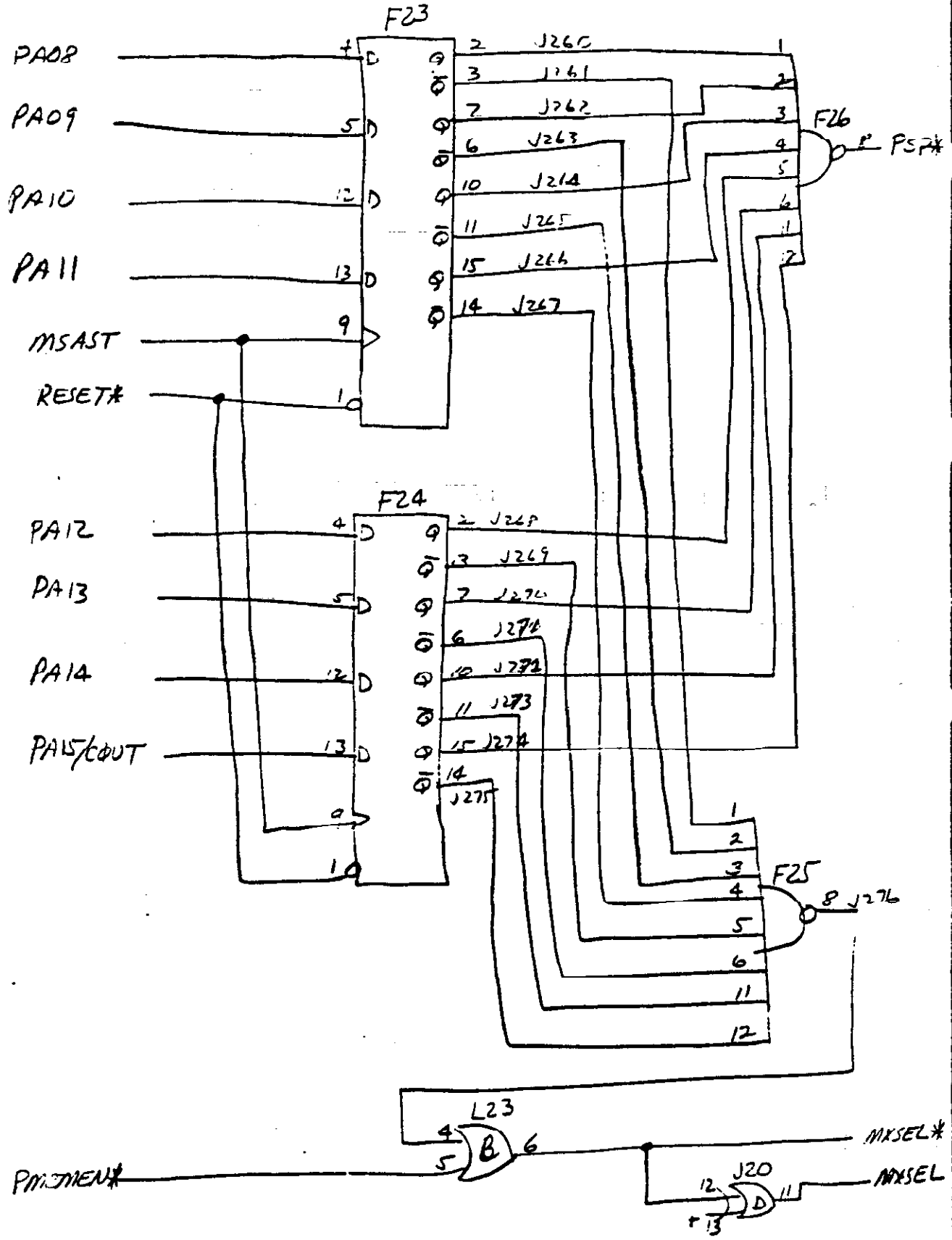
ALC Data Bus, HSK, BAV



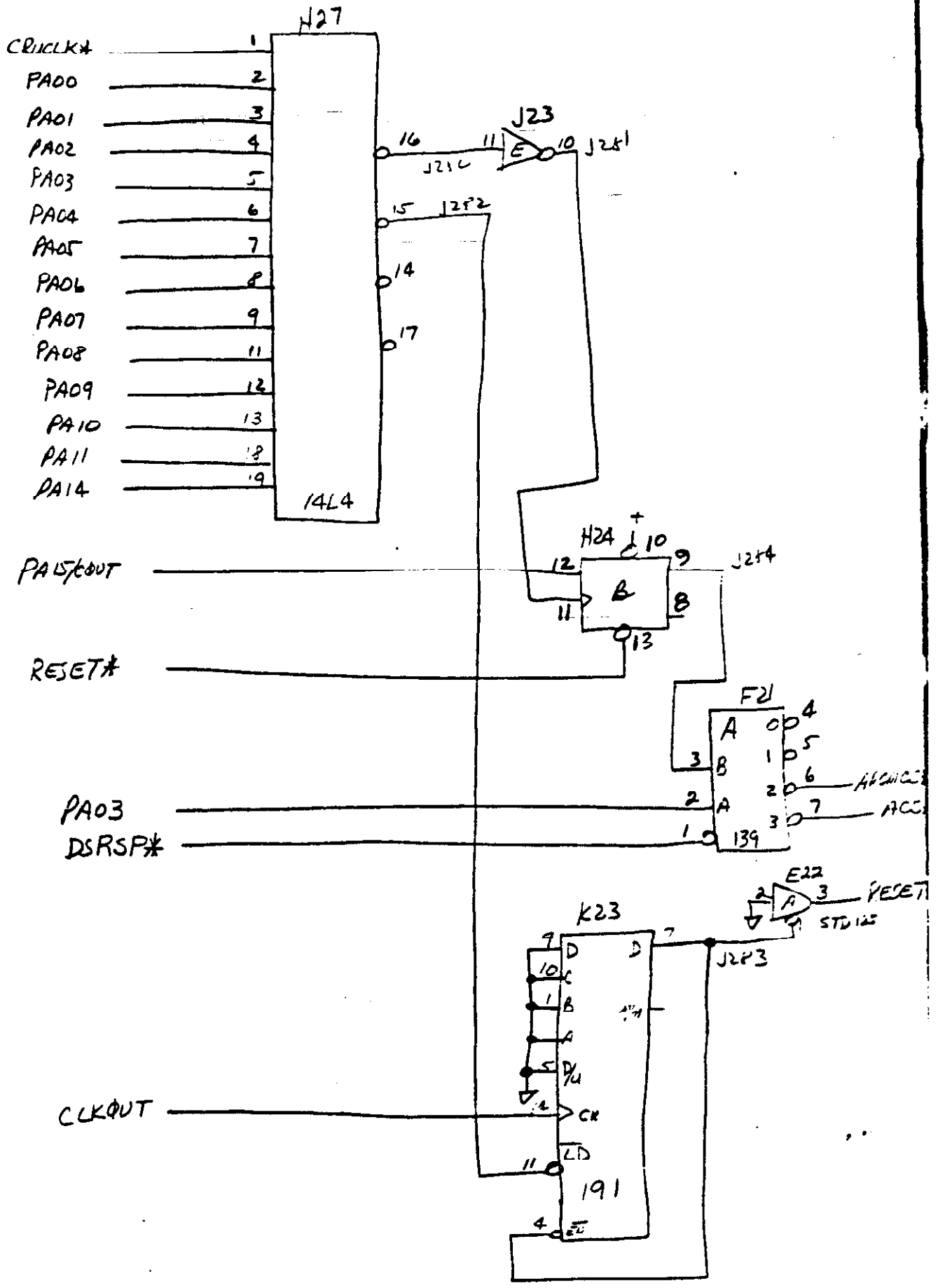
Control Log. Unit HSK Section Logic



ALL

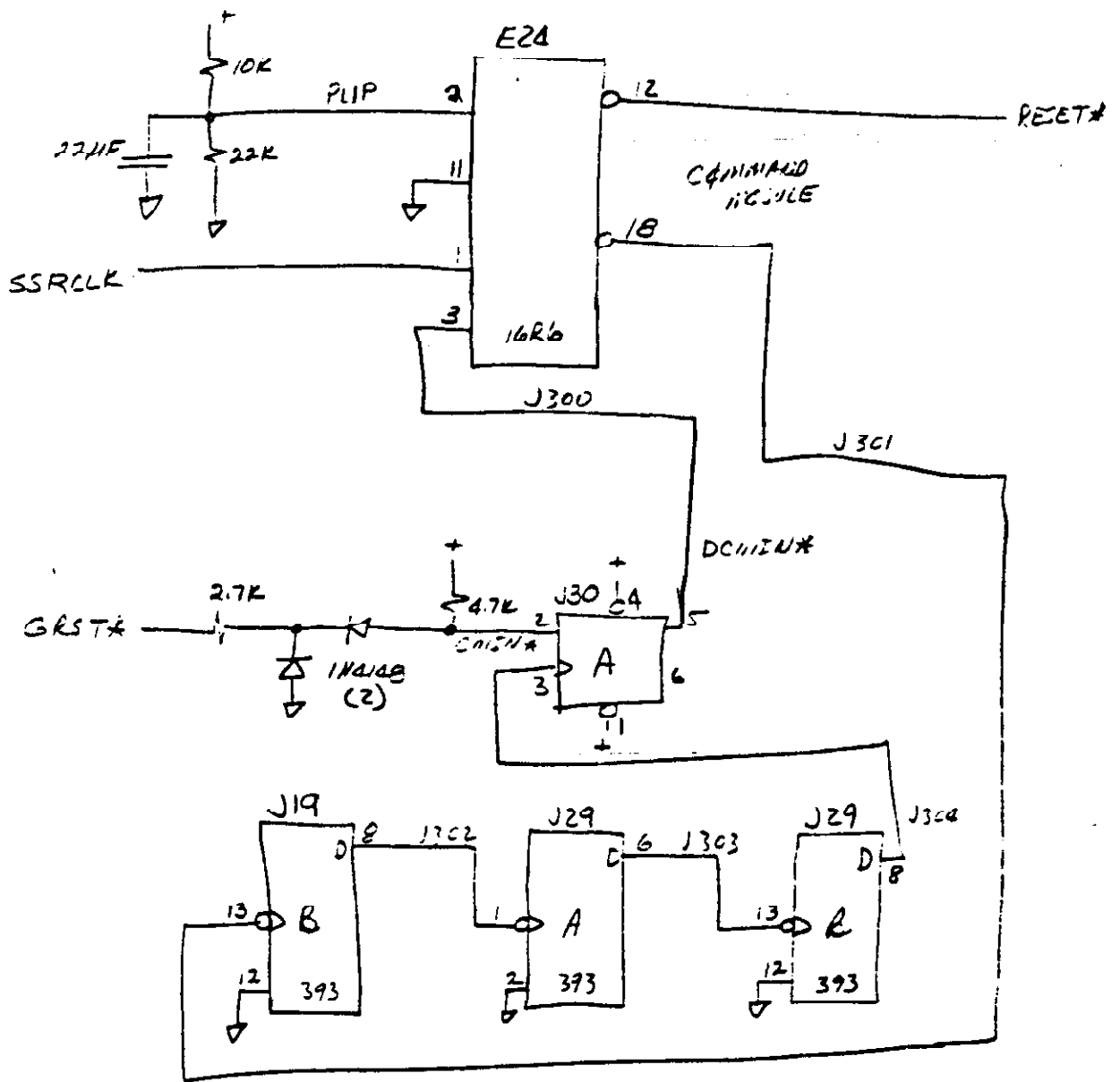


PAs Decode

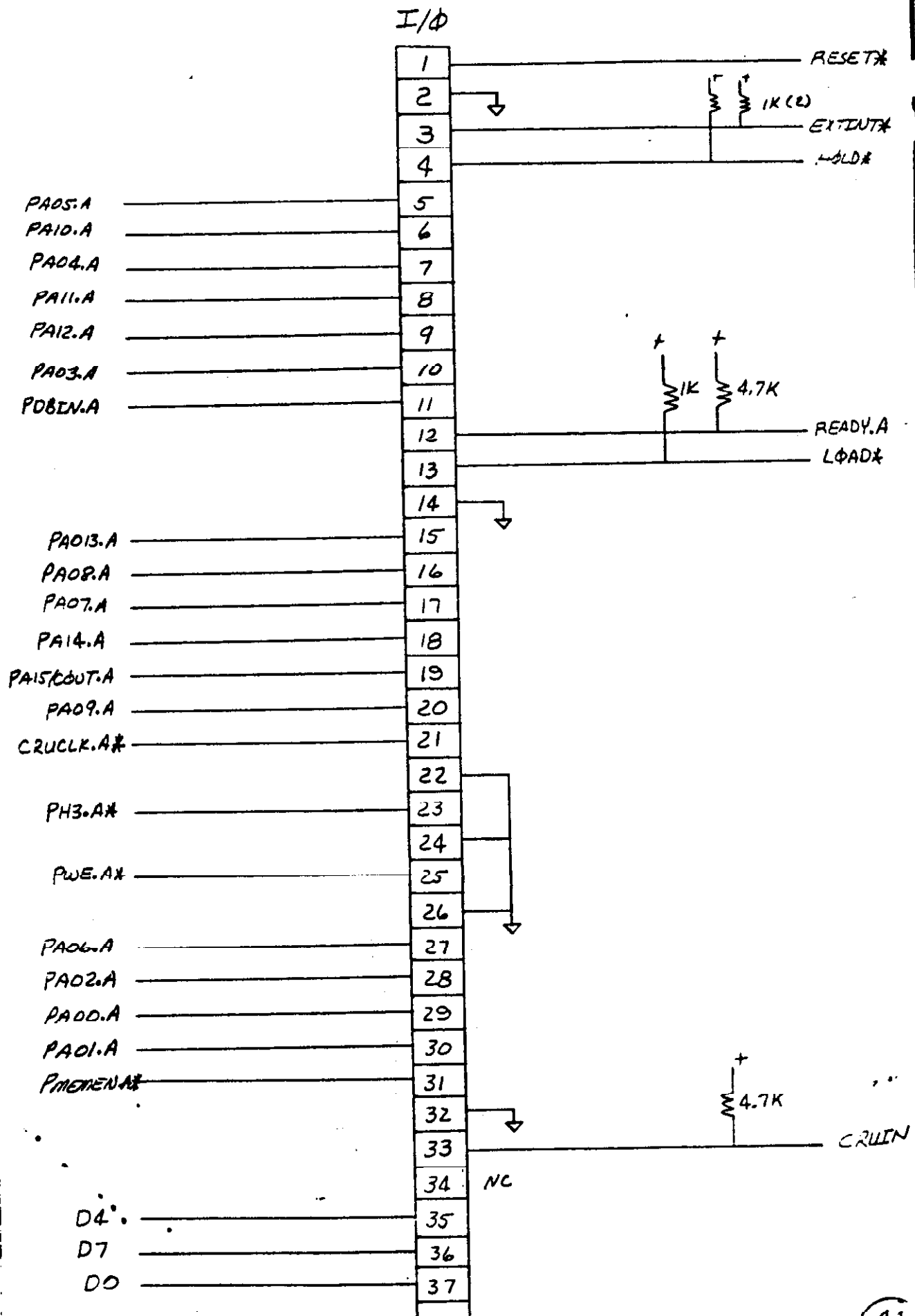


CRU DECODES

(1)



COMMAND MODULE RESET



I/O CONN