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GENERAL DESCRIPTION

The concept for the Texas Instruments Home Computer 99/4 I/O bus is to provide maximum flexibility and good performance within a constraint of low cost for both mainframe and computer system. This concept is achieved by providing both memory and CRU I/O buses to the 99/4 peripherals. This brief description will give key details of this interface. Detailed information regarding the 9900 CPU is assumed. A source for this information is the 9900 Family Systems Design and Data Book. This manual may be obtained from TI Semiconductor Distribers. The memory bus (with data bus converted to eight bits wide) is used for instruction fetch from ROM in external peripherals and for data transfer to/from memory mapped portions of these devices. The CRU bus is used for peripheral enable/disable and for device control and data transfer to/from CRU mapped peripherals.

A block diagram of the TI 99/4 electronics is shown in Figure A. The TMS 9900 microprocessor accesses each peripheral to obtain instructions from the device service routine (DSR) read only memory. Since each peripheral contains its own DSR, the 99/4 does not have to be designed to anticipate future peripheral requirements. The dual I/O bus capability, along with interupt handling and external DSR's provide flexibility at low cost.

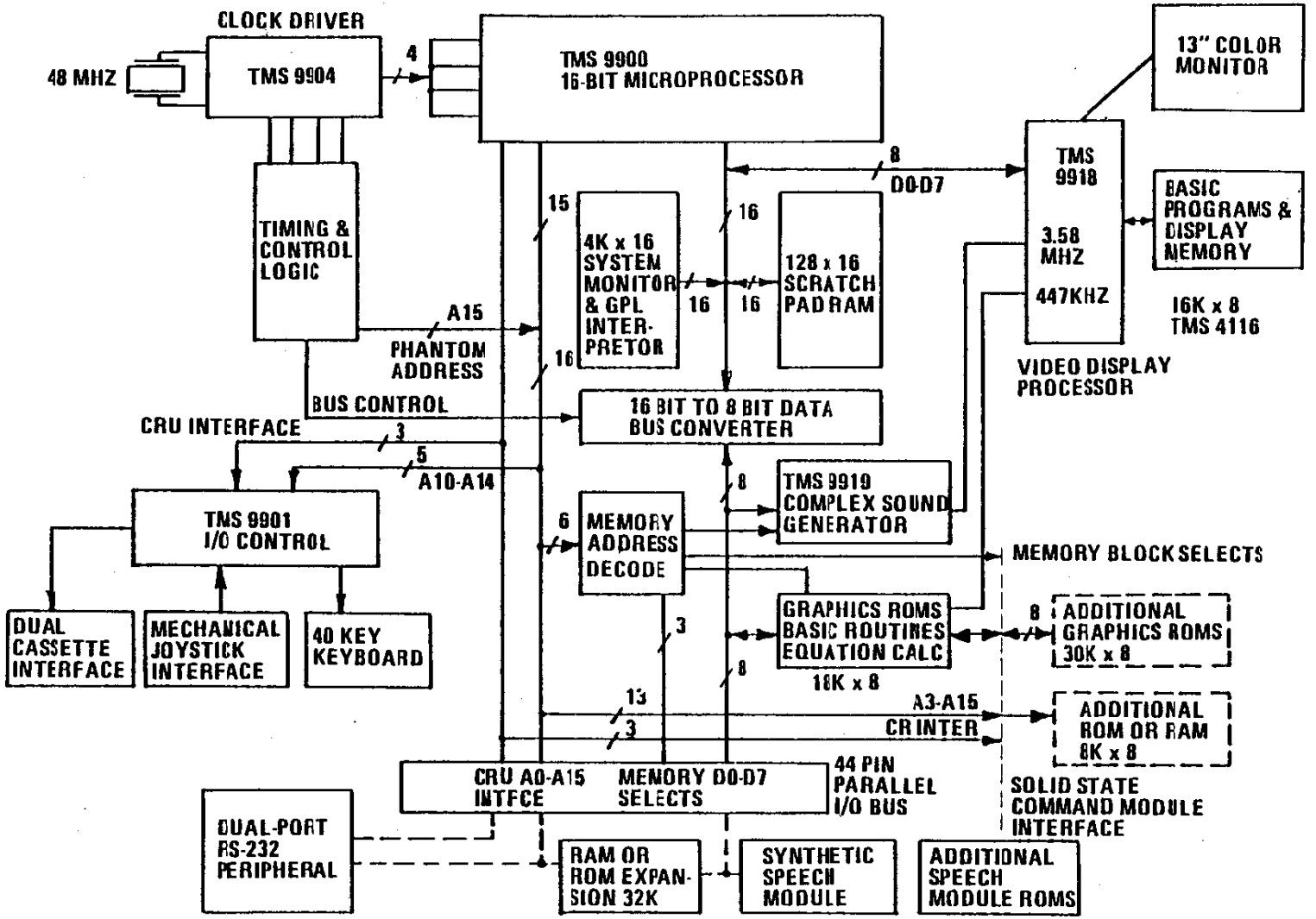


FIGURE A

99/4 SYSTEM BLOCK DIAGRAM

I. I/O PIN DESCRIPTION

SIGNATURE	PIN	I/O	DESCRIPTION
AØ (MSB)	31	Out	
A1	30	Out	ADDRESS BUS
A2	20	Out	
A3	10	Out	A0 through A15 comprise the address bus. This bus provides the 16 bit memory address vector to the external memory system when MEMEN is active. Address bit 15 is also used for CRU DATA OUT on CRU output instructions.
A4	7	Out	
A5	5	Out	
A6	29	Out	
A7	17	Out	
A8	14	Out	
A9	18	Out	
A10	6	Out	
A11	8	Out	
A12	11	Out	
A13	15	Out	
A14	16	Out	
A15/CRUOUT	19	Out	
DØ (MSB)	37	I/O	DATA BUS
D1	40	I/O	
D2	39	I/O	D0 through D7 comprise the bidirectional data bus. This bus transferes memory data to (when writing) and from (when reading) the external memory system when MEMEN is active.
D3	42	I/O	
D4	35	I/O	
D5	38	I/O	
D6	36	I/O	
D7	34	I/O	
			BUS CONTROL
MEMEN	32	Out	MEMory ENable. MEMEN indicates a memory access.
DBIN	9	Out	Data Bus In. When active (high) the data buffers and 9900 are in the input mode.
WE	26	Out	Write ENable. WE indicates a memory write.
MBE	28	Out	Memory Block Enable. MBE indicates a memory access in memory block 4000-5FFF.
CRUCLK	22	Out	CRU Clock. Indicates data is available on the CRU OUT line.
CRUIN	33	In	CRU data IN. Input data line to the Home Computer.

I/O PIN DESCRIPTION (CONTINUED)

SIGNATURE	PIN	I/O	DESCRIPTION
			MEMORY CONTROL
READY/$\overline{\text{HOLD}}$	12	In	READY (when $\overline{\text{MEMEN}}$ is active) indicates external memory is ready for a memory access. HOLD (when $\overline{\text{MEMEN}}$ is inactive) indicates a request to use the data bus.
HOLDA/IAQ	41	Out	HOLD Acknowledge goes true when $\overline{\text{MEMEN}}$ is inactive and indicates that the 9900 is in a HOLD state. Instruction AcQuisition indicates (when $\overline{\text{MEMEN}}$ is active) the CPU is acquiring an instruction during a memory cycle.
			TIMING AND CONTROL
$\overline{\text{LOAD}}$	13	In	When active, LOAD cuases the CPU to execute a nonmaskable interrupt with memory address FFFC containing the trap vector.
$\overline{\text{RESET}}$	3	Out	When active, RESET causes the Home Computer and the peripherals to be reset. Will be held active for a minimum of 5 clock cycles.
EXT INT	4	In	EXTernal INTerrupt. When active, EXT INT causes the CPU to execute an interrupt.
Ø3	24	Out	CPU Clock. Phase 3 of the CPU clock.
			POWER
GND	21,23 25,27		Ground reference.
			SPEECH MODULE SIGNALS
$\overline{\text{SBE}}$	2	Out	Speech Block Enable. $\overline{\text{SBE}}$ indicates a memory access in the speech memory.
AUDIO IN	44	In	Input for the audio from the speech module.

+5	1	Supply voltage (+5V Nom) for speech module (50ma Max)
-5	43	Supply voltage (-5V Nom) for speech module (50ma Max)

II. MEMORY ALLOCATION

The memory address space is broken into 8 blocks of 8K bytes of memory. The third block (addresses 4000 - 5FFF) is predecoded and made available at the I/O port for the peripherals. The sixth, seventh and eighth block (addresses A000 - FFFF) are available for future expansion. For the speech module, (addresses 9000 - 97FF), a predecoded line is available at the I/O port.

SYSTEM MEMORY MAP

HEX ADDRESS

0 - 1FFF	Console ROM Space
2000 - 3FFF	Future Expansion (internal/console)
4000 - 5FFF	Peripheral expansion (predecoded to I/O Connector)
6000 - 7FFF	Game cartridge ROM/RAM (predecoded to GROM Connector)
8000 - 9FFF	Microprocessor RAM, VDP, GROM, SOUND and SPEECH select.
A000 - BFFF	Future Expansion
C000 - DFFF	Future Expansion
E000 - FFFF	Future Expansion

MEMORY MAPPED DEVICES

ADDRESSES	A0	A1	A2	A3	A4	A5	A14	A15	USE
8000	1	0	0	0	0	0	0	0	Internal RAM (8300-83FF)
8400	1	0	0	0	0	1	0	0	Sound
8800	1	0	0	0	1	0	0	0	VDP Read Data
8802	1	0	0	0	1	0	1	0	VDP Read Status
8C00	1	0	0	0	1	1	0	0	VDP Write Data
8C02	1	0	0	0	1	1	1	0	VDP Write Address
9000	1	0	0	1	0	0	0	0	Speech Read
9400	1	0	0	1	0	1	0	0	Speech Write
9800	1	0	0	1	1	0	0	0	GROM Read Data
9802	1	0	0	1	1	0	1	0	GROM Read Address
9C00	1	0	0	1	1	1	0	0	GROM Write Data
9C02	1	0	0	1	1	1	1	0	GROM Write Address

III. CRU ALLOCATION

Of the available 4K of CRU bits, the first 1K (addresses 0000-07FE) are used internally in the Home Computer. The second 1K (addresses 0800-0FFE) are reserved for future use. The last 2K (addresses 1000-1FFE) are reserved for the peripherals to be plugged in the I/O port. A block of 128 CRU bits is assigned to each peripheral as listed below.

CRU ASSIGNMENTS

CRU ADDRESSES	A3	A4	A5	A6	A7	USE
0000-0FFE	0	X	X	X	X	INTERNAL USE
1000-10FE	1	0	0	0	0	RESERVED
1100-11FE	1	0	0	0	1	DISK CONTROLLER
1200-12FE	1	0	0	1	0	RESERVED
1300-13FE	1	0	0	1	1	RS 232 (I)
1400-14FE	1	0	1	0	0	RESERVED
1500-15FE	1	0	1	0	1	RS 232 (II)
1600-16FE	1	0	1	1	0	RESERVED
1700-17FE	1	0	1	1	1	RESERVED
1800-18FE	1	1	0	0	0	THERMAL PRINTER
1900-1FFE	1	1	X	X	X	FUTURE EXPANSION

IV. INTERRUPT HANDLING

The interrupt available on the I/O port is one of the maskable interrupts of the TMS 9901 Programmable Systems Interface.

9900 INTERRUPTS

INTERRUPT LEVEL	VECTOR LOC. (MEMORY ADDR. IN HEX)	CPU PIN	DEVICE ASSIGNMENT
(Highest Priority) 0	0000	RESET	RESET
1	FFFC	LOAD	LOAD
	0004	INT1	EXT DEV (9901)

Lower priority CPU interrupts are not used. The additional interrupts available are implemented on 9901.

9901 INTERRUPT MAPPING

ADDRESS	CRU BIT	9901	PIN	FUNCTION
0000	0	Control		Control
0002	1	INT1	17	External
004C	2	INT2	18	Video Display Processor Vertical Sync
0006	3	INT3	9	CLock Interrupt, Keyboard "ENTER" line, Joystick "FIRE"
0008	4	INT4	8	Keyboard "L" line, Joystick "Left"
000A	5	INT5	7	Keyboard "P" line, Joystick "Right"
000C	6	INT6	6	Keyboard "0" line, Joystick "Down"
000E	7	INT7 (P15)	34	Keyboard "SHIFT" line, Joystick "UP"
0010	8	INT8 (P14)	33	Keyboard space line
0012	9	INT9 (P13)	32	Keyboard "Q" line
0014	10	INT10 (P12)	31	Keyboard "1" line
0016	11	INT11 (P11)	30	Not Used
0018	12	INT12 (P12)	29	Reserved
001A-1E	13-15	INT13-INT15	28,27 & 23	Not Used

9901 I/O MAPPING

ADDRESS	CRU BIT	9901	PIN	FUNCTION
0020	16	P0	38	Reserved
0022	17	P1	37	Reserved
0024	18	P2	26	BIT_2 (LSB) of Keyboard Select
0026	19	P3	22	Bit_1 of Keyboard Select
0028	20	P4	21	Bit_0 (MSB) of Keyboard Select
002A	21	P5	20	Not used
002C	22	P6	19	Cassette Control 1
002E	23	P7 (INT15)	23	Cassette Control 2
0030	24	P8 (INT14)	27	Audio Gate
0032	25	P10(INT12)	28	Mag Tape Out
0036	27	P11(INT11)	30	Mag Tape Input
0038-003E	28-31	P12-P15	31-34	Not Used

V. ELECTRICAL CHARACTERISTICS

DRIVE CAPABILITY OF I/O SIGNALS

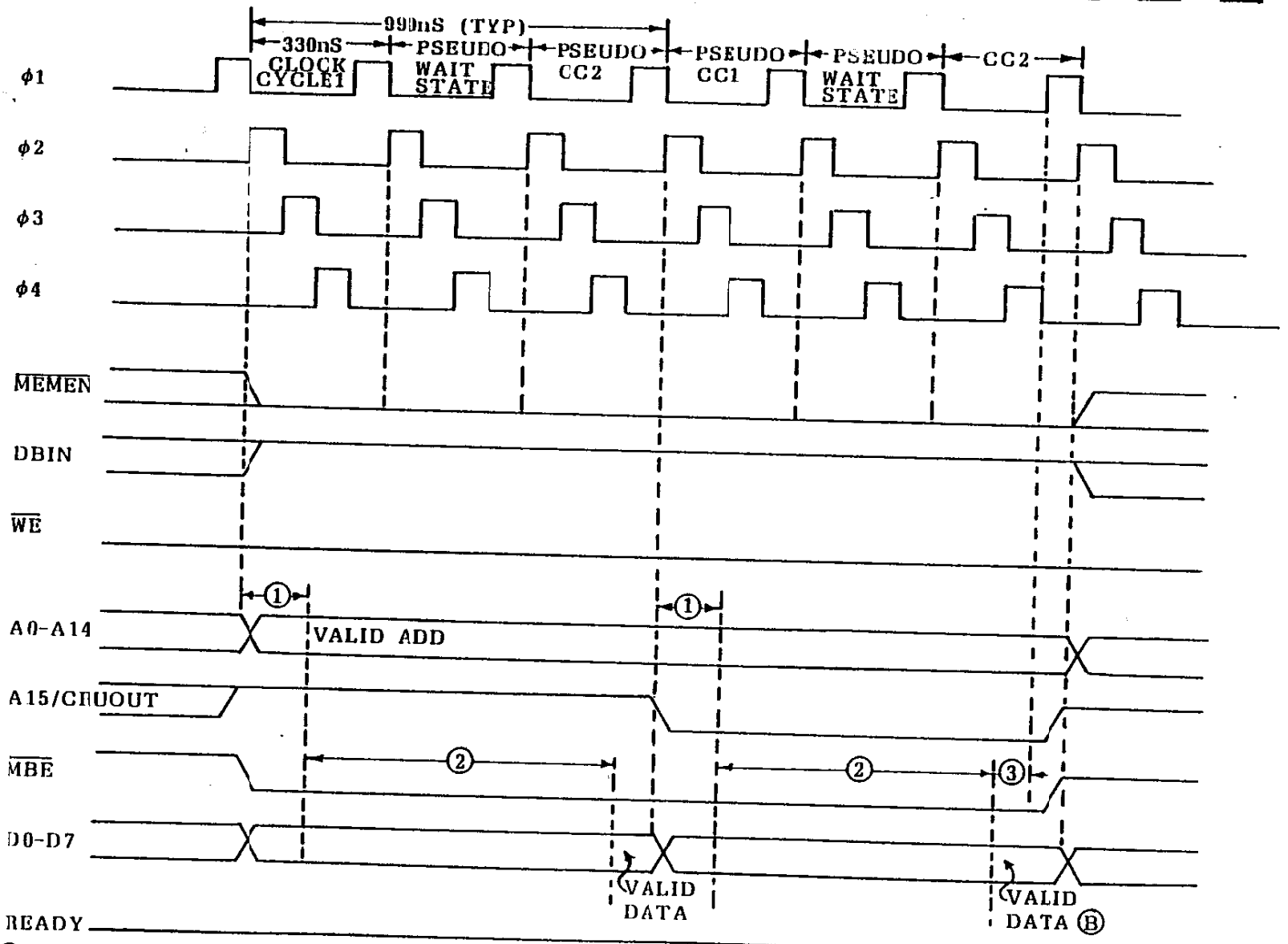
SIGNAL NAME	DRIVER
$\overline{Ø3}$	74LS244
CRUCLK	74LS244
$\overline{WE}$	74LS244
A0	74LS244
A1	74LS244
DBIN	74LS244
$\overline{MBE}$	74LS138
MEMEN	74LS32
A3-A14	74LS367
D0-D7	74LS245
A15/CRUOUT	74LS244
SBE	74LS03
HOLDA	74LS32
$\overline{RESET}$	74LS04

I/O READ

A CPU Read cycle for the external device consists of two 8-bit read cycles (Fig. B). The 2 bytes read are assembled as a 16 bit word before they are presented to the 9900. Shown in Fig. B are two 8 bit read cycles with one wait state inserted in each to work with slow memories. MEMEN goes low true at the beginning of clock cycle 1. At the same time DBIN goes high true. $\overline{WE}$ stays high false during the entire cycle. At the same time that MEMEN goes true, the address bus goes active. In order for the noise and the glitches (associated with crosstalk and simultaneous switching) to go away a minimum of 100nS should be allowed for the address lines to settle. $\overline{MBE}$ (precoded from A0, A1 and A2) goes true during the leading edge of Ø2 of clock cycle 1. Data read from the peripherals will be valid 750nS after the start of clock cycle 1. The CPU will look at the full 16 bit data bus during the leading edge of Ø1, of clock cycle 2. Under worse-case conditions, data must be valid 100nS before that time.

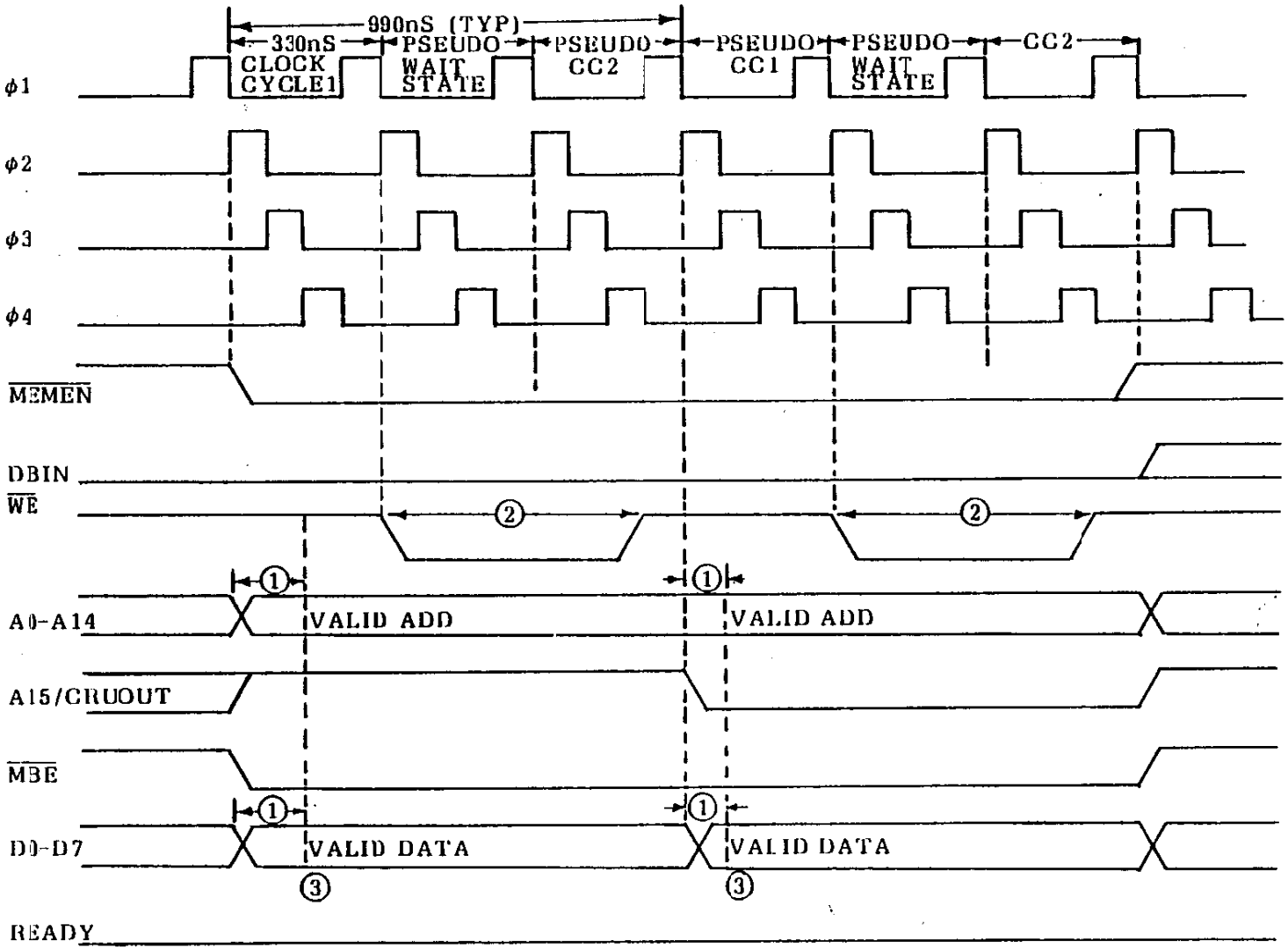
I/O WRITE

Figure C shows a 16 bit I/O write cycle. As described earlier it is composed of two 8-bit writes. A write cycle will always be preceeded by an ALU cycle. MEMEN and DBIN go true at the start of the cycle. A settling time of 100nS (min) is allowed for the address lines to settle down. $\overline{WE}$



①-SETTLING TIME= 100nS (MIN)
②-ACCESS TIME FOR DSR ROM + DATA Ts + DATA BUFF DELAY (PEREFERAL + MAINFRAME) =650nS (MAX)
③-SETUP TIME FOR 9900= 60nS (MIN)

FIGURE B
I/O READ TIMING



①-SETTLING TIME= 100nS (MIN)
②-$\overline{WE}$ PULSE WIDTH= 660nS (TYP)
③-VALID DATA

FIRURE C

I/O WRITE TIMING

I/O WRITE (CONT)

goes true (low) on the leading edge of Ø2, during the wait states, and stays true for 660nS (TYP). Both during a Read or a Write the odd byte is accessed first, followed by the even byte. A15/CRU OUT changes its state 900nS (TYP) after the cycle is initiated. The second 8-bit write cycle is identical to the first 8-bit write. $\overline{\text{MBE}}$ stays true (low) during the entire (1.8us) cycle.

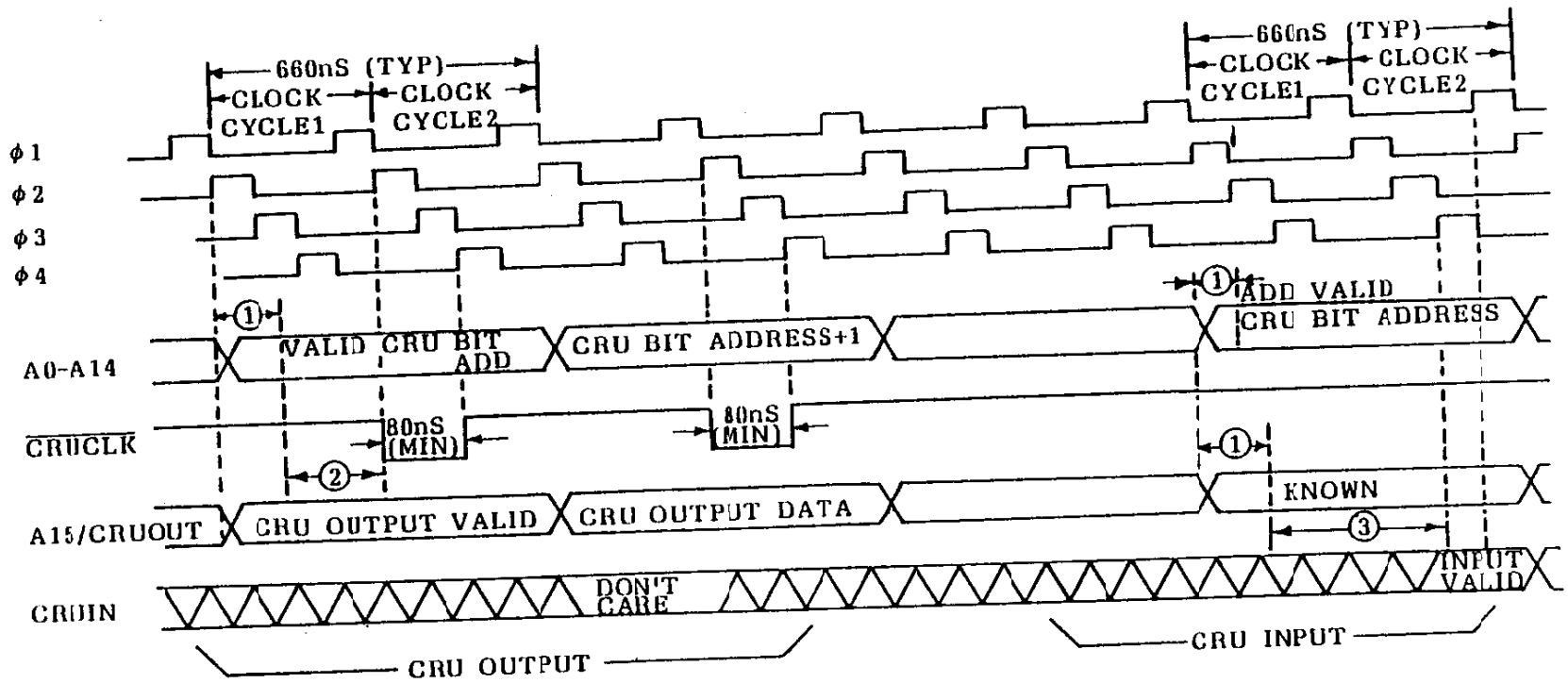
CRU TIMING

CRU interface timing is shown in Figure D. The CRU OUT cycle is composed of 2 clock cycles. The CRU bit address when placed on the address bus A0 through A14 is allowed to settle for 100nS (min). CRUCLK is a 80nS (min) low true signal which occurs on the trailing edge of Ø1 of clock cycle 2. CRUOUT data is valid at the start of clock cycle 1, and is latched by the CRUCLK in the respective peripheral.

CRUIN also consists of 2 clock cycles 660nS (TYP). Again we allow 100nS for the address bus to settle down. The CPU samples the CRUIN line on the leading edge of Ø1 of clock cycle 2. Data must be valid 40nS (min) before that.

I/O BUS LOADING

SIGNAL	TOTAL SWITCHING LOAD (pF)	MAXIMUM PERIPHERAL LOAD (pF)
D0-D7	210	90
A0-A2	100	90
A3-A14	100	90
CRUOUT/A15	110	100
$\overline{\text{Ø3}}$	110	100
$\overline{\text{RESET}}$	100	90
READY/HOLD	80	70
CRUIN	125	90
$\overline{\text{CRUCLK}}$	100	90
$\overline{\text{MBE}}$	100	90
$\overline{\text{WE}}$	100	90
$\overline{\text{SBE}}$	35	25
$\overline{\text{DBIN}}$	100	90
$\overline{\text{MEMEN}}$	100	90
HOLDA/IAQ	80	70



①-SETTLING TIME 100nS (MIN)
②-ADD VALID TO $\overline{\text{CRUCLK}}$ =220nS (TYP)
③-ADD VALID TO VALID CRUIN =400nS (MAX)

FIGURE D

CRU TIMING

VI. GLOSSARY

CPU	Central Processing Unit
CRU	Communication Register Unit (I/O technique for TMS 9900 Microprocessor)
DSR	Device Service Routine (TMS 9900 machine language).
GROM	Graphics read only memory (TMC 0430). This memory device is a 6144 byte read only memory with on board 14 bit program counter. The program counter can be written or read through an eight bit interface and will automatically autoincrement.
I/O	Input/Output.
VDP	Video Display Processor (TMS 9918).

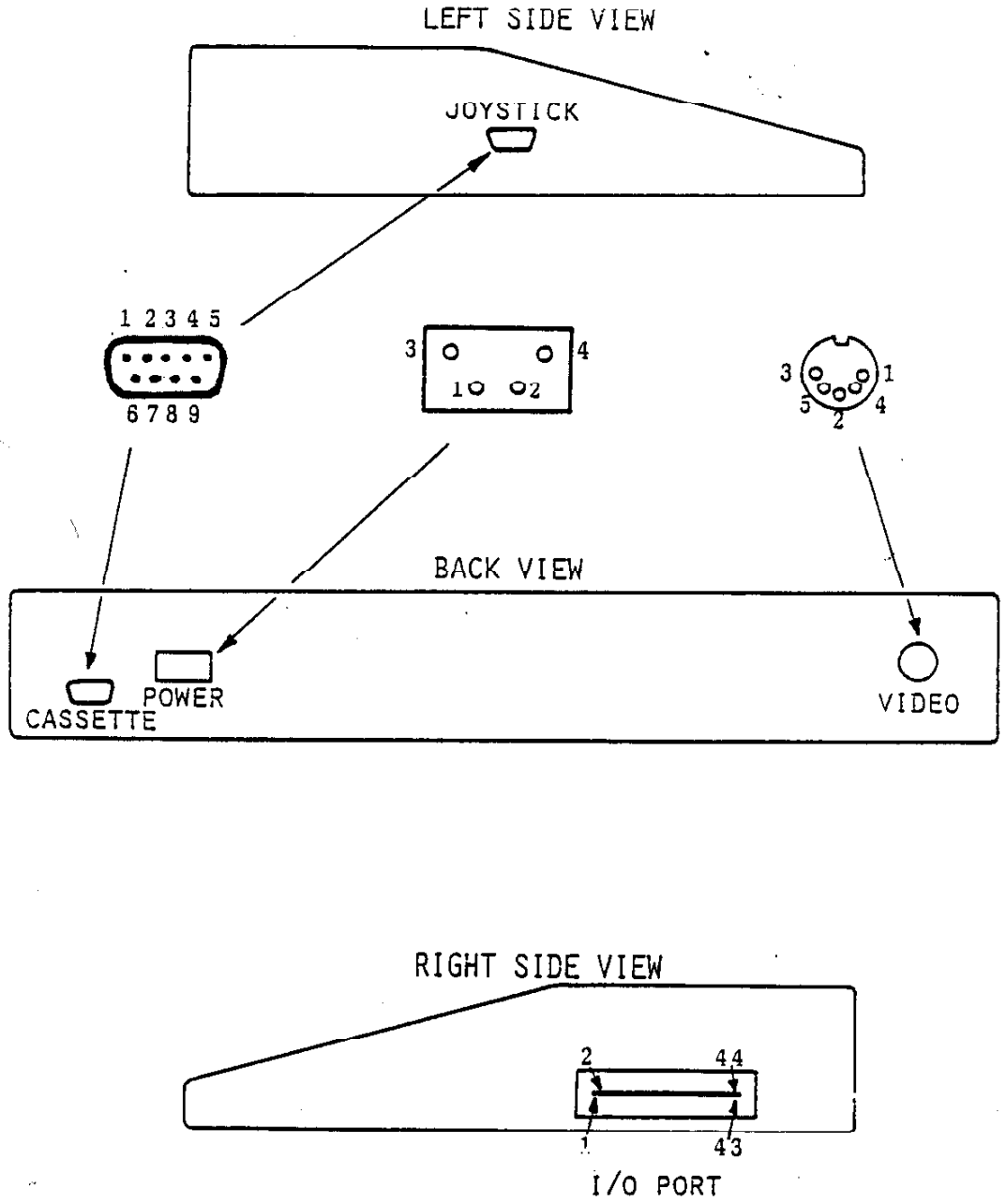


FIGURE E
CONNECTOR PIN IDENTIFICATION DIAGRAM

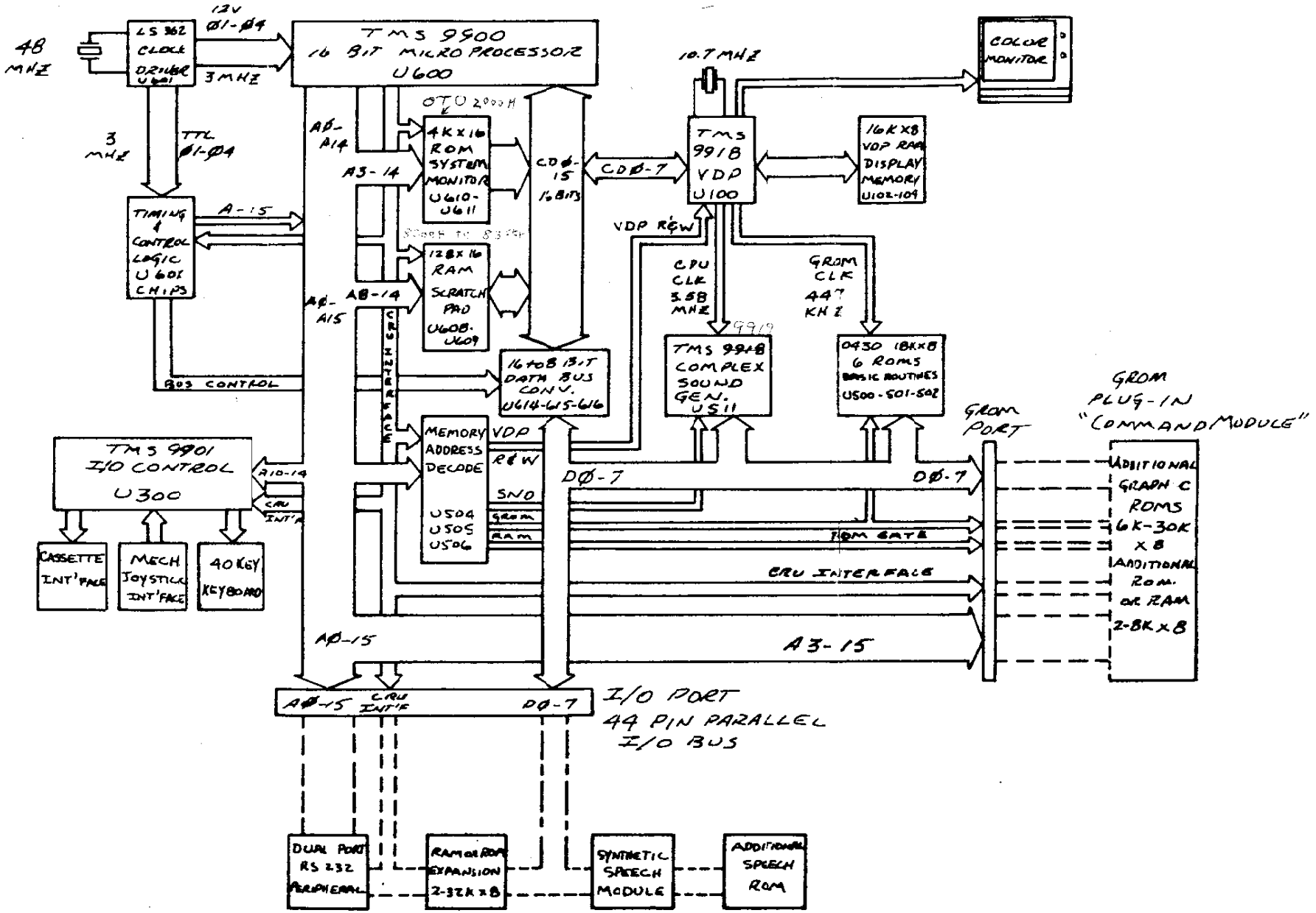
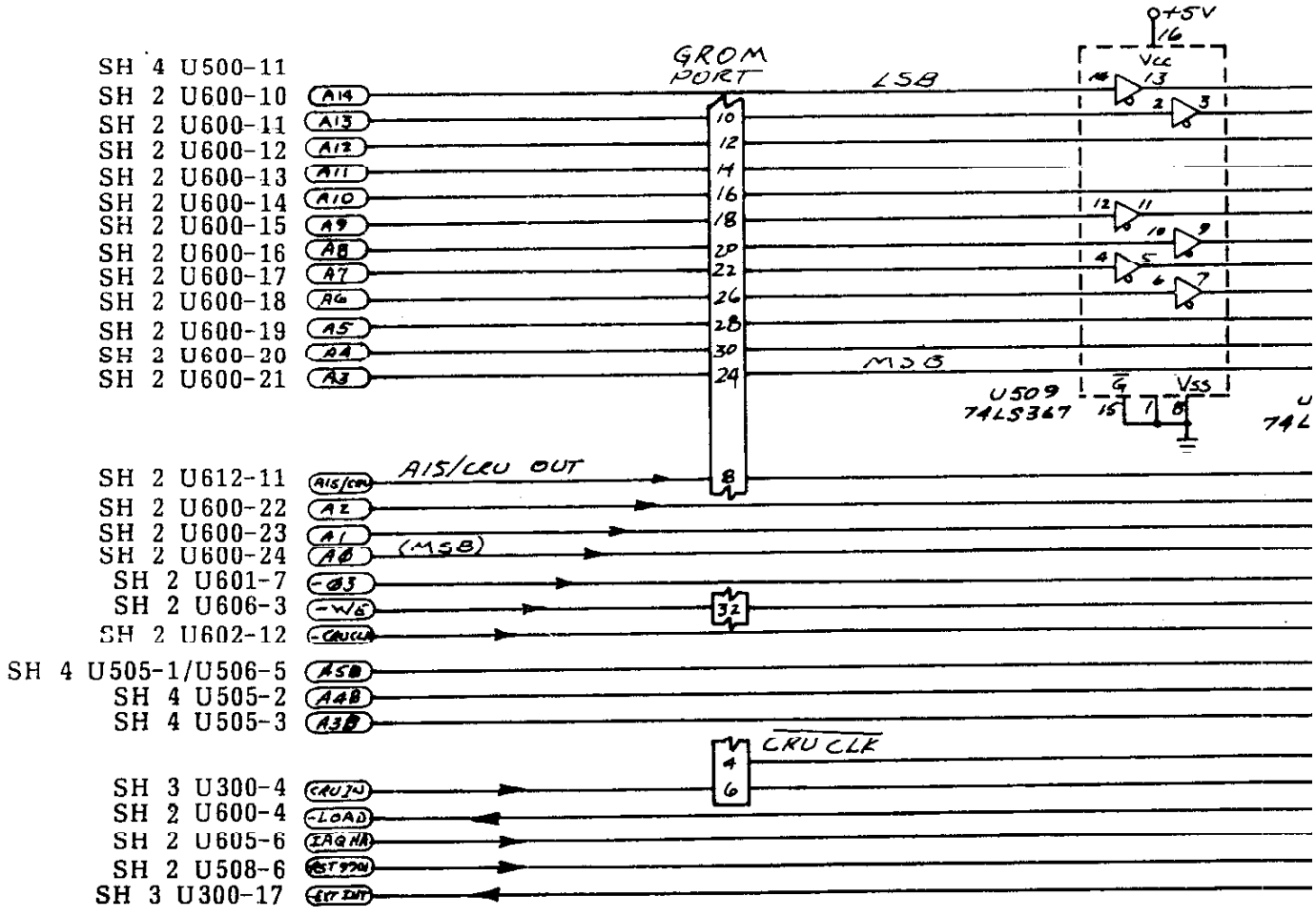


FIGURE G
99/4 SCHEMATIC DIAGRAM
(SHEET 6 OF 6)


GROM PORT
LSB
MSB
+5V
Vcc
U509
74LS367
Vss
A15/CRU OUT
(MSB)
CRU CLK
SH 4 U500-11
SH 2 U600-10
SH 2 U600-11
SH 2 U600-12
SH 2 U600-13
SH 2 U600-14
SH 2 U600-15
SH 2 U600-16
SH 2 U600-17
SH 2 U600-18
SH 2 U600-19
SH 2 U600-20
SH 2 U600-21
SH 2 U612-11
SH 2 U600-22
SH 2 U600-23
SH 2 U600-24
SH 2 U601-7
SH 2 U606-3
SH 2 U602-12
SH 4 U505-1/U506-5
SH 4 U505-2
SH 4 U505-3
SH 3 U300-4
SH 2 U600-4
SH 2 U605-6
SH 2 U508-6
SH 3 U300-17

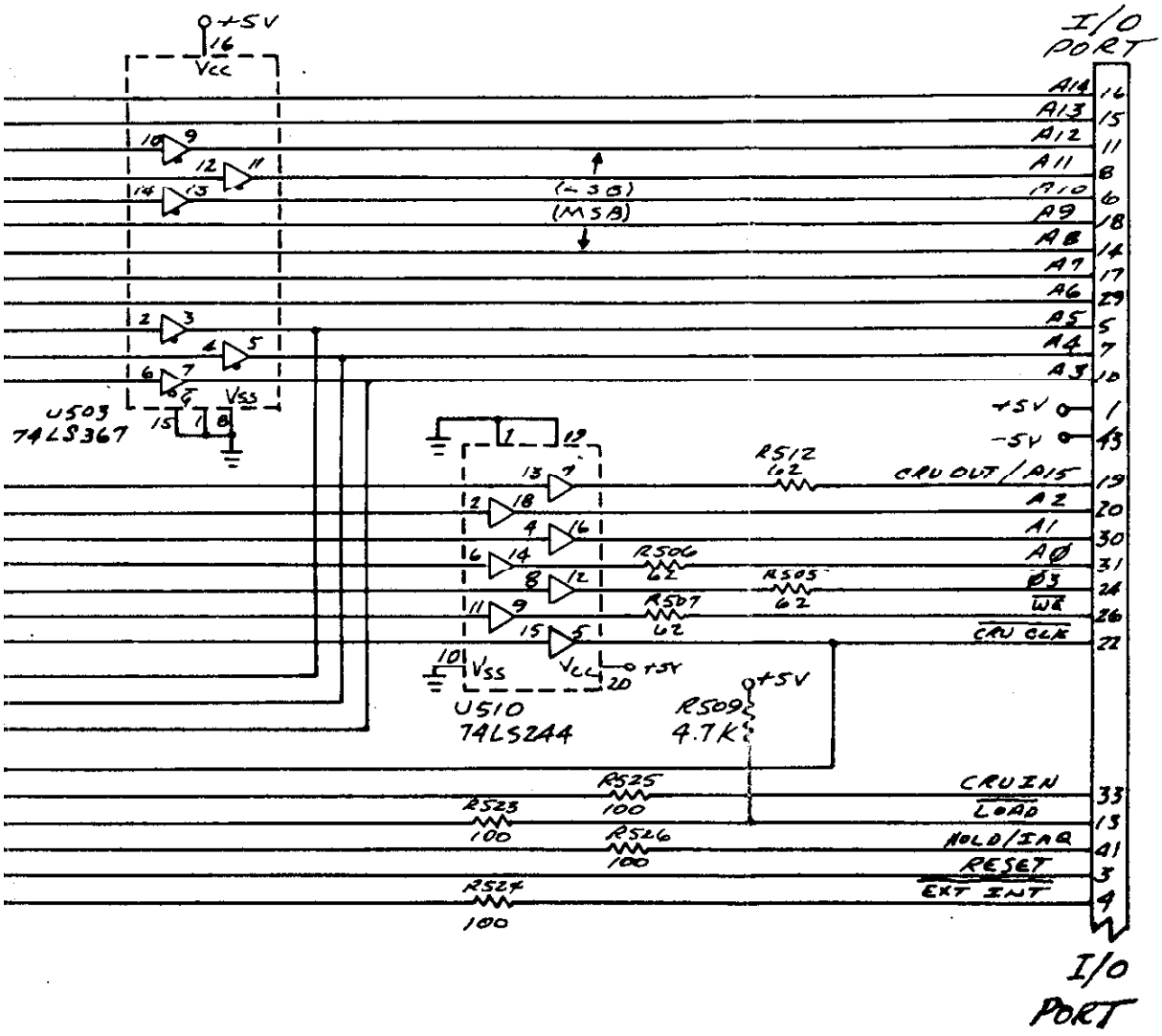
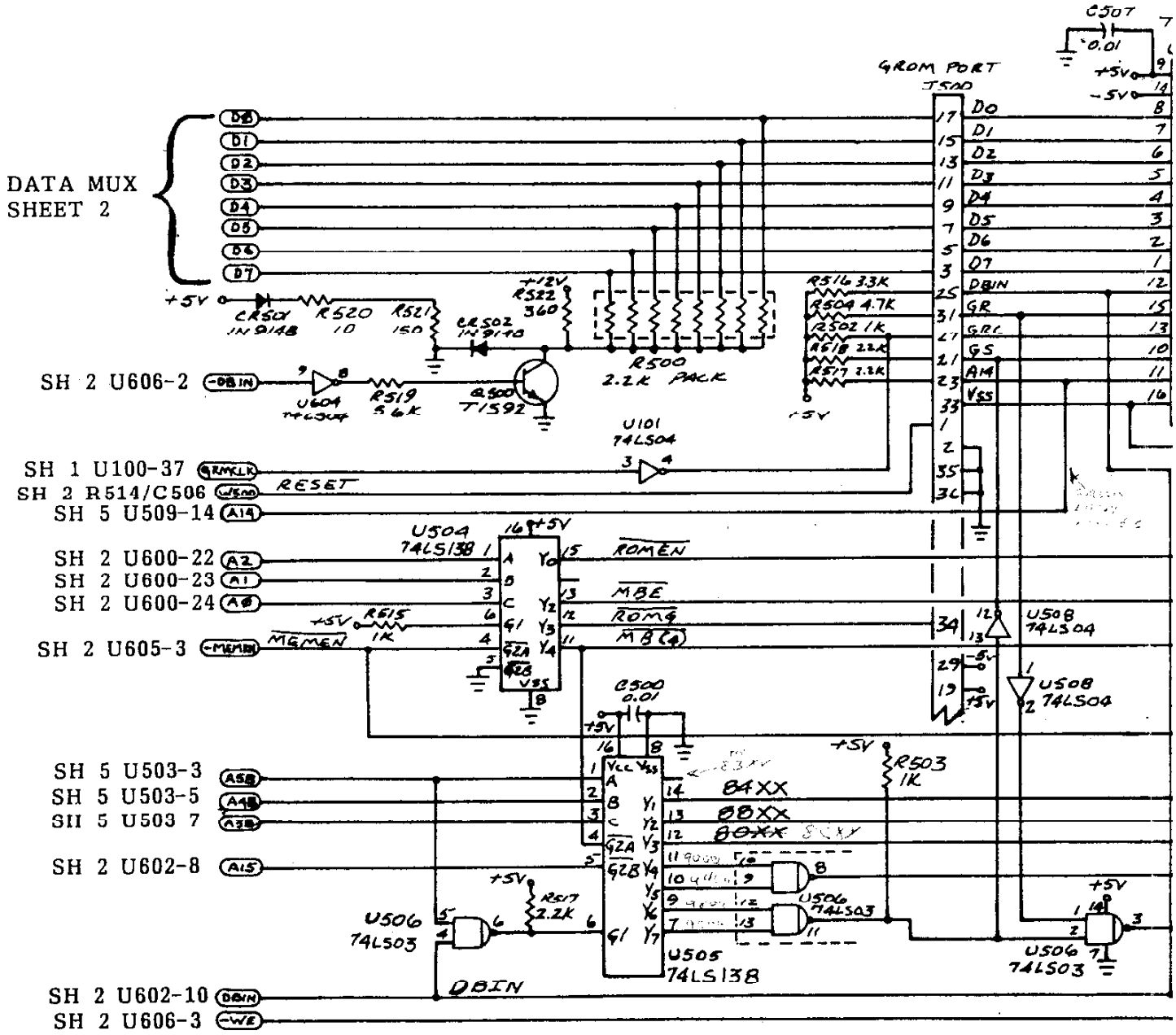


FIGURE G
99/4 SCHEMATIC DIAGRAM
(SHEET 5 OF 6)


DATA MUX
SHEET 2
SH 2 U606-2
SH 1 U100-37
SH 2 R514/C506
SH 5 U509-14
SH 2 U600-22
SH 2 U600-23
SH 2 U600-24
SH 2 U605-3
SH 5 U503-3
SH 5 U503-5
SH 5 U503 7
SH 2 U602-8
SH 2 U602-10
SH 2 U606-3
GROM PORT
J500
U504
74LS138
U505
74LS138
U506
74LS03
U508
74LS04
U101
74LS04
R500
2.2K PACK
R503
1K
C500
0.01
C507
0.01
RESET
ROMEN
MBE
ROMG
MB(4)
MEMEN
DBIN
84XX
88XX
80XX

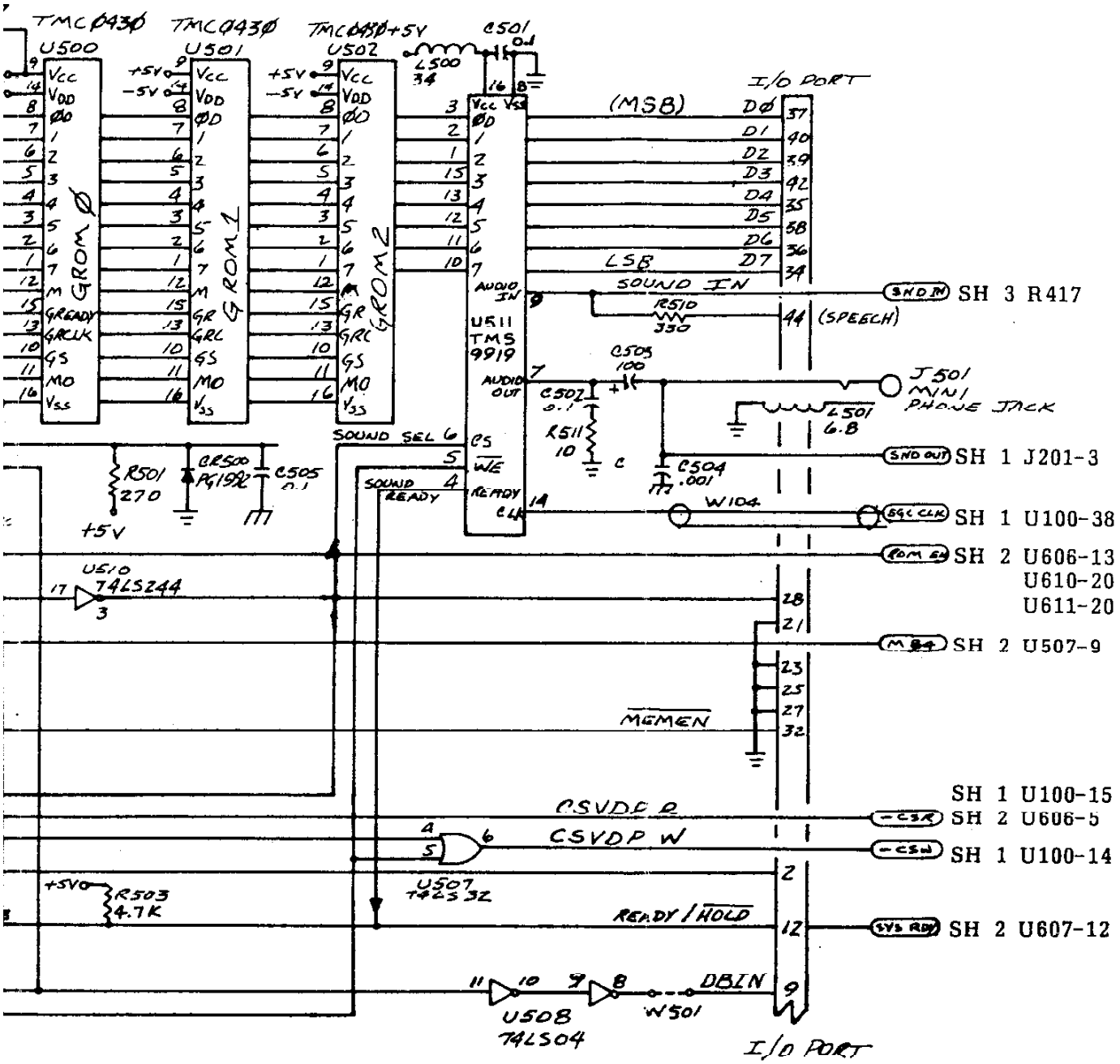
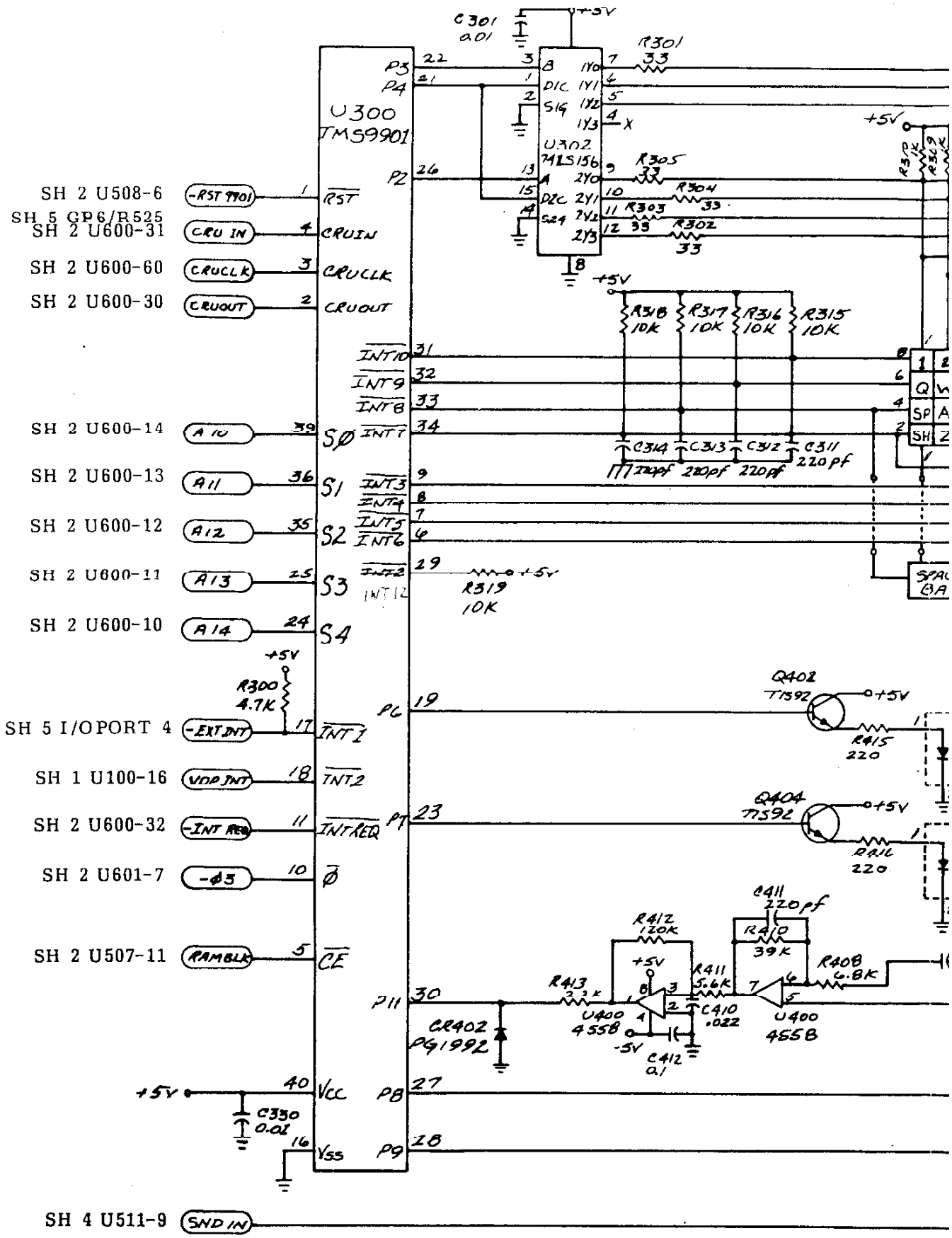


FIGURE G
99/4 SCHEMATIC DIAGRAM
(SHEET 4 OF 6)


U300
TMS9901
U302
74LS156
SH 2 U508-6
-RST 9901
SH 5 GP6/R525
SH 2 U600-31
CRU IN
SH 2 U600-60
CRUCLK
SH 2 U600-30
CRUOUT
SH 2 U600-14
A10
SH 2 U600-13
A11
SH 2 U600-12
A12
SH 2 U600-11
A13
SH 2 U600-10
A14
SH 5 I/OPORT 4
-EXT INT
SH 1 U100-16
VDP INT
SH 2 U600-32
-INT REQ
SH 2 U601-7
-Ø3
SH 2 U507-11
RAMBLK
SH 4 U511-9
SND IN
C301
0.01
R301
33
R305
33
R304
33
R303
33
R302
33
R306
10K
R307
10K
R308
10K
R309
10K
C314
220pf
C313
220pf
C312
220pf
C311
220pf
R319
10K
R300
4.7K
Q402
TI592
R415
220
Q404
TI592
R416
220
C411
220pf
R412
120K
R410
39K
R408
0.8K
R413
2.2K
R411
5.6K
C410
.022
U400
455B
CR402
PG1992
C412
.01
C330
0.01

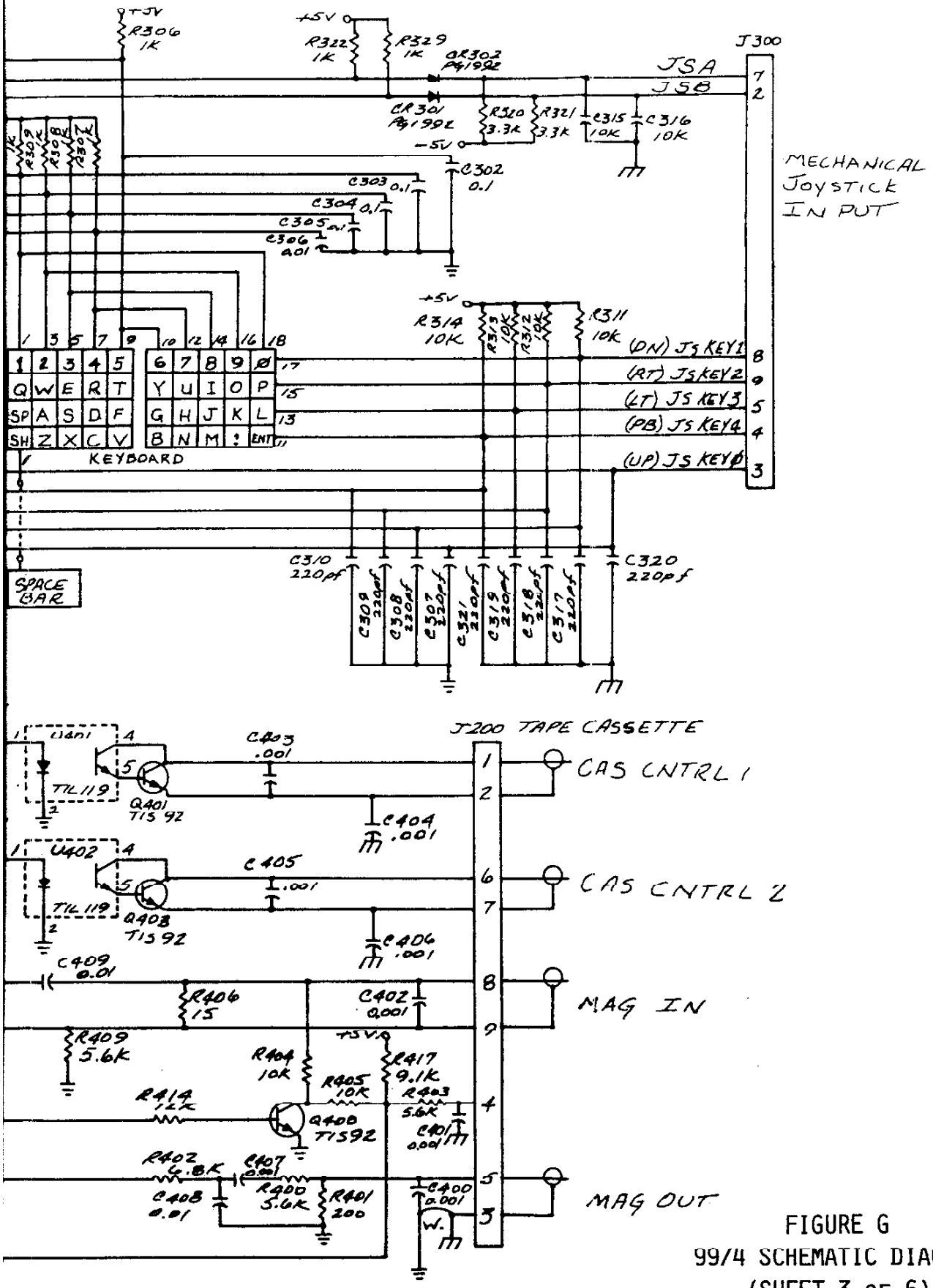
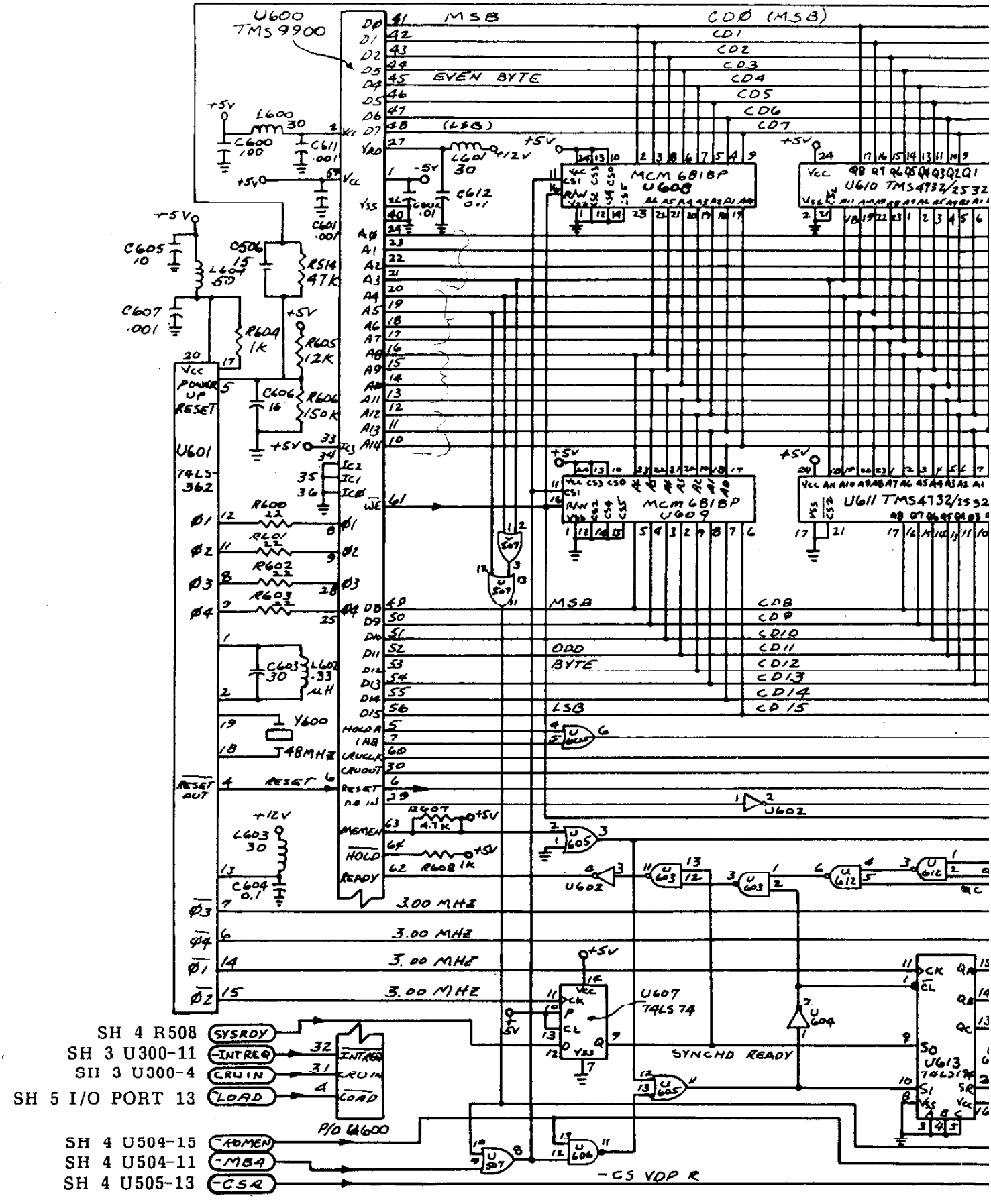


FIGURE G
99/4 SCHEMATIC DIAGRAM
(SHEET 3 OF 6)


U600
TMS9900
MSB
EVEN BYTE
(LSB)
CD0 (MSB)
CD1
CD2
CD3
CD4
CD5
CD6
CD7
MCM 6818P
U608
U609
U610 TMS4732/2532
U611 TMS4732/2532
U601
74LS362
POWER UP RESET
RESET OUT
RESET
HOLD
READY
MEMEN
WE
ODD BYTE
LSB
CD8
CD9
CD10
CD11
CD12
CD13
CD14
CD15
Y600
48MHZ
3.00 MHZ
U607
74LS74
SYNCHD READY
U613
74LS174
SH 4 R508 SYSRDY
SH 3 U300-11 -INTREQ
SH 3 U300-4 CRUIN
SH 5 I/O PORT 13 LOAD
P/O U600
SH 4 U504-15 -MDMEN
SH 4 U504-11 -MB4
SH 5 U505-13 -CSR
-CS VDP R

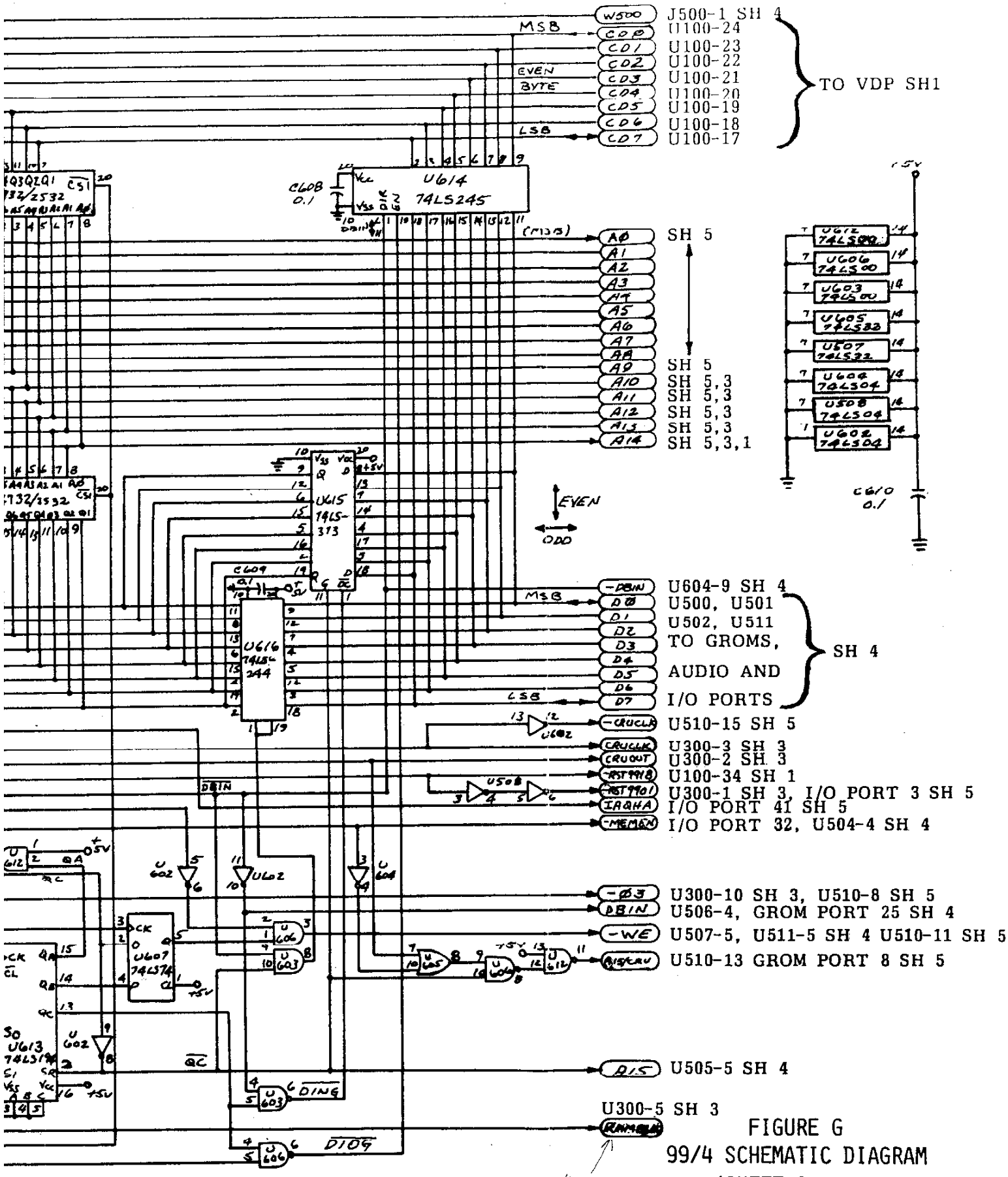
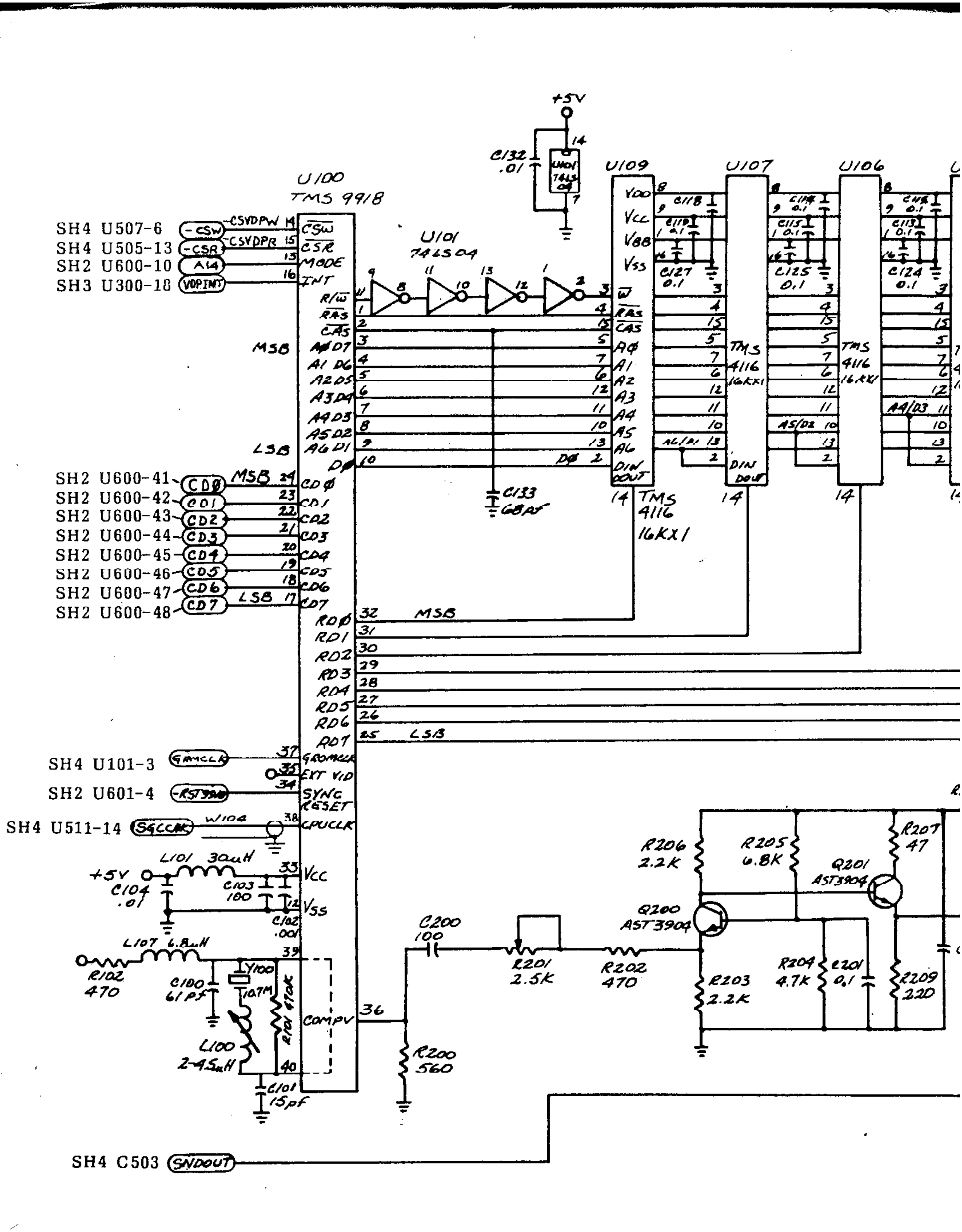


FIGURE G
99/4 SCHEMATIC DIAGRAM
(SHEET 2 OF 6)


+5V
C132 .01
U101 74LS04
U100 TMS 9918
U109
U107
U106
SH4 U507-6
-CSW
CSVDPW
SH4 U505-13
-CSR
CSVDPR
SH2 U600-10
A14
SH3 U300-18
VDPINT
CSW
CSR
MODE
INT
R/W
RAS
CAS
MSB
LSB
A0 D7
A1 D6
A2 D5
A3 D4
A4 D3
A5 D2
A6 D1
D0
VDD
VCC
VBB
VSS
C118
C119
C127 0.1
C114 0.1
C115 0.1
C125 0.1
C116 0.1
C113 0.1
C124 0.1
W
DIN
DOUT
TMS 4116 16KX1
C133 68pF
SH2 U600-41
SH2 U600-42
SH2 U600-43
SH2 U600-44
SH2 U600-45
SH2 U600-46
SH2 U600-47
SH2 U600-48
CD0
CD1
CD2
CD3
CD4
CD5
CD6
CD7
RD0
RD1
RD2
RD3
RD4
RD5
RD6
RD7
SH4 U101-3
GROMCLK
EXT VID
SH2 U601-4
-RST99
SYNC RESET
SH4 U511-14
SGCCLK
W104
CPUCLK
L101 30uH
+5V
C104 .01
C103 100
C102 .001
VCC
VSS
L107 6.8uH
R102 470
C100 61pF
Y100 10.7M
R101 470K
L100 2-4.5uH
C101 15pF
COMPV
C200 100
R201 2.5K
R202 470
R200 560
R206 2.2K
R205 6.8K
R207 47
Q201 AST3904
Q200 AST3904
R203 2.2K
R204 4.7K
C201 0.1
R209 220
SH4 C503
SNDOUT

NOTES
UNLESS OTHERWISE SPECIFIED:
1. RESISTORS ARE IN OHMS
2. CAPACITORS ARE IN MICROFARADS
3. COILS ARE IN MILLIHENRIES

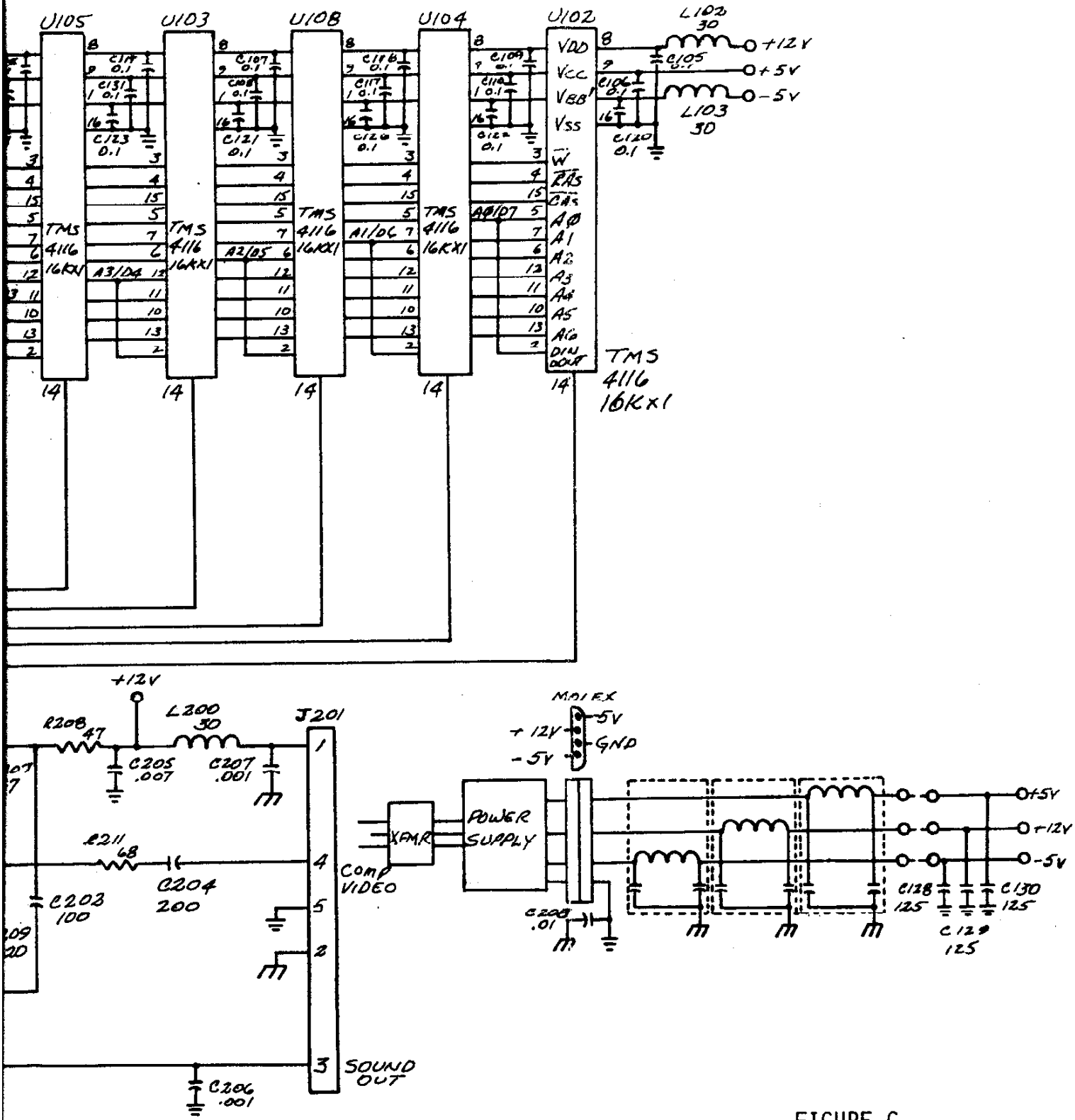
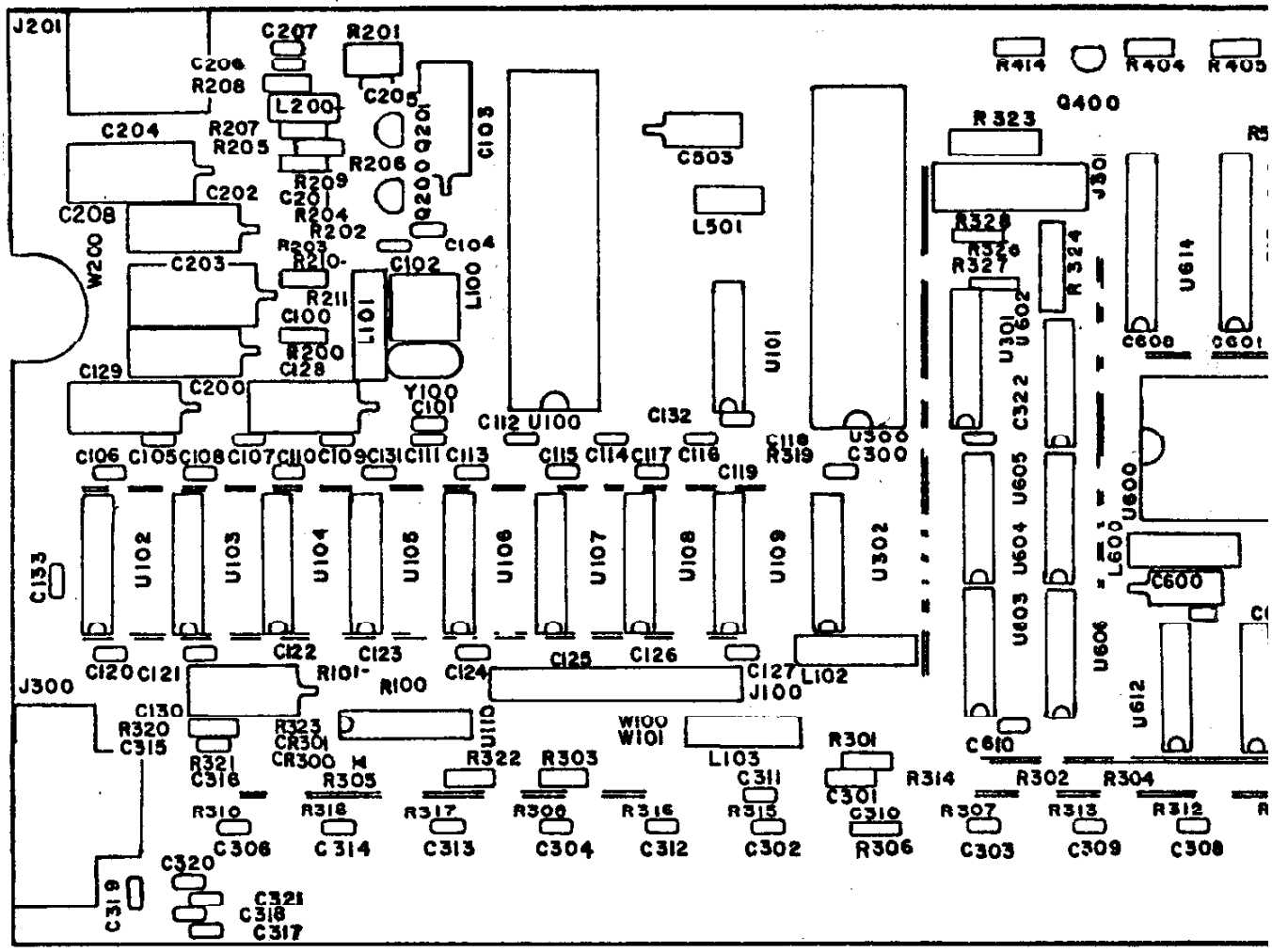


FIGURE G
99/4 SCHEMATIC DIAGRAM
(SHEET 1 OF 6)


J201
C207
R201
C206
R208
L200
C205
C204
R207
R205
R206
C202
R209
C201
R204
C208
R202
R203
R210
C104
C102
C203
R211
C100
R200
C128
C129
C200
Y100
C101
C112
U100
C132
C118
R319
U300
C300
C106
C105
C108
C107
C110
C109
C131
C111
C113
C115
C114
C117
C116
C119
C133
U102
U103
U104
U105
U106
U107
U108
U109
U302
C120
C121
C122
C123
C124
C125
C126
C127
L102
J100
J300
C130
R320
C315
R321
C316
R323
CR301
CR300
R305
R101
R100
C110
R322
R303
W100
W101
L103
C311
R301
C301
R314
R302
R304
R310
C306
R318
C314
R317
C313
R308
C304
R316
C312
R315
C302
C310
R306
R307
C303
R313
C309
R312
C308
C320
C321
C318
C317
C319
R414
R404
R405
Q400
R323
C803
L501
U101
R328
R326
R327
R324
U301
U602
C322
U614
C608
C601
U605
U604
U603
U606
U600
L600
C600
C610
U612

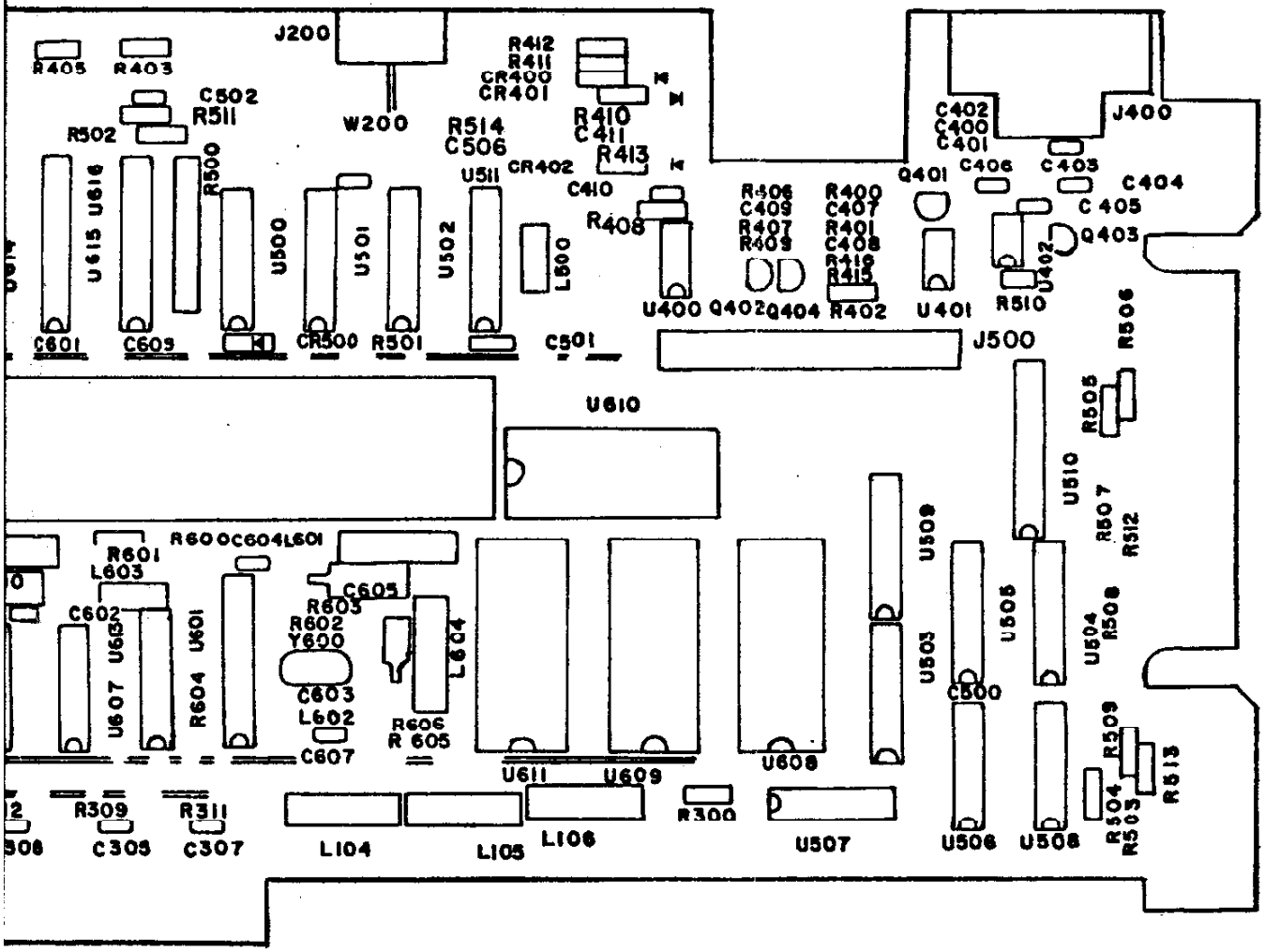


FIGURE F
99/4 LOGIC BOARD
COMPONENT LOCATION DIAGRAM